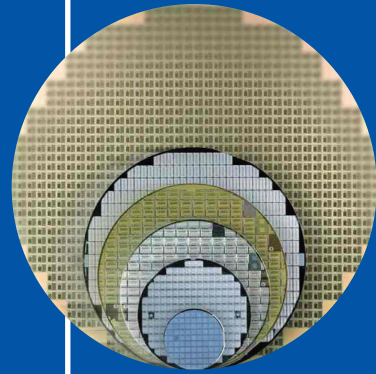


2007

Strategic Research Agenda

European Nanoelectronics Initiative Advisory Council

Strategic Research Agenda

European Technology Platform Nanoelectronics

Second Edition, November 2007

Preface

Nanoelectronics is the essential hardware enabler for electronic product and service innovation in key growth markets for European industry, such as telecommunications, transportation and medical technology. ENIAC, the European Technology Platform for Nanoelectronics, was launched in 2004 with the overall aim to guarantee Europe the earliest possible access to leading-edge integrated components and design skills for application in high-technology products and services, thereby reinforcing Europe's existing industrial strengths and ensuring that core intellectual property is generated and benefited from in the region.

The ENIAC Strategic Research Agenda (SRA) is created through the concerted efforts of experts from industry, academia, and public authorities across Europe. Top executives of leading European companies and research organisations have signalled their full commitment to reaching the ambitious goals set out by the SRA and the Joint Technology Initiative in Nanoelectronics proposed by the European Commission.

This Second Edition of the ENIAC SRA is a full revision of the First Edition that was presented on November 23, 2005, in Barcelona. Starting from an overall vision of the global and European landscape between now and 2020, the Agenda defines the critical societal needs and lead markets that are enabled by Nanoelectronics. These applications are then translated and detailed into priorities for each of the technology domains underpinning the Nanoelectronics research challenge. The Agenda concludes with a critical assessment of the European ecosystem and puts forward proposals for moving forward towards full realisation of the ENIAC ambitions. It is planned to continue issuing revisions every two years.

Dr Wolfgang Ziebart
President of the AENEAS Association
Chairman of the ENIAC Steering Committee

Budapest, November 28, 2007

Content

5 Executive summary

7 Vision
7 Cornerstone industry
7 Global value chain evolution
8 Europe 2020

10 Societal needs and lead markets
10 Introduction
11 Health and wellness
12 Transport and mobility
12 Security and safety
13 Energy and environment
14 Communication
15 Infotainment
16 Conclusion

17 Technology domains
17 Introduction
18 More Moore
24 More than Moore
34 Heterogeneous Integration
36 Beyond CMOS
44 Design Methods and Tools
50 Equipment and Materials
57 Conclusion

59 European ecosystem
59 Opportunities and threats
59 Stakeholder roles

61 Making it happen
61 Mobilising Europe
61 Roadmap for partnership

63 Acknowledgement

63 References

Executive summary

The global semiconductor industry underpins a sixth of the world's total economy and re-invests up to 20% of its revenue into research and development. These two facts alone make it a cornerstone industry for any region that wants to remain at the forefront of the knowledge economy.

The new era of nanoelectronics is enabling an exponential increase in system complexity and functionality. However, it has also brought with it exponential increases in capital expenditure and knowledge requirement. In response, the semiconductor industry has de-verticalised, moving from linear supply chains to a series of interconnected ecosystems that leverage the economic benefits of resource sharing. Application knowledge has become the main differentiator for market success.

Within the context of the revised Lisbon Strategy, a market-oriented approach based on the identification of lead markets for innovative products and services has been proposed as the best way of reinforcing Europe's ambitions to become a highly competitive, dynamic, full-employment knowledge-based economy. ENIAC's mission is to direct the future of nanoelectronics R&D in order to realise those ambitions. Societally relevant lead markets in which nanoelectronics will make an important contribution lie in areas such as Health and Wellness, Transport and Mobility, Security and Safety, Energy and Environment, Communications and Infotainment.

However, in many cases, market success depends on consumer acceptance of new ideas. The introduction of new products and services therefore carries considerable risk, and there is a danger that it will lead to reduced R&D expenditures, restricting technological development. Yet rapid and continuous technological progress remains critical for achieving Europe's ambitions.

Although the success or failure of individual products and services is difficult to predict, the underlying technology trends needed for rapid progress in nanoelectronics are less so. The most obvious of these is ensuring the continuation of Moore's Law - the prediction that the cost-per-transistor on a silicon chip will halve every two to three years. Although this technology domain, commonly referred to as 'More Moore', continues to target reduction of device dimensions in next-generation CMOS processes, it increasingly also includes the development of new processes and materials that improve device performance.

Home to some of the world's leading research institutes in semiconductor physics, Europe's expertise in the More Moore domain is on a par with the rest of the world. Europe is also home to highly successful multinational chip manufacturers and CMOS manufacturing plants. It has particular expertise in building value-added options on top of CMOS semiconductor processes, such as high-voltage and power handling, that will keep Europe's existing wafer fabs in production and maintain its highly skilled workforce.

Even if European semiconductor companies eventually adopt fab-lite production models, the need to engineer these value-added options makes it critical for Europe to maintain its leading-edge semiconductor R&D, with the increasing involvement of academia. For example, European researchers must have networked access to leading-edge infrastructures that can handle 300-mm diameter silicon wafers, requiring strong financial support at the European level to complement national and/or industrial initiatives. Greater cooperation with leading research organisations outside Europe should also be encouraged and nanoelectronics education within Europe will need to be enhanced.

In addition to creating value-added options, European R&D will increasingly turn its attention to extending the 'More than Moore' domain - creating semiconductor-based devices that convert real-world non-digital as well as non-electronic information such as mechanical, thermal, acoustic, chemical, optical and biomedical phenomena to and from the digital domain. Development of these devices is critical to all the lead markets that Europe will target with nanoelectronics. In many cases, they can be produced in Europe's existing wafer fabs, further extending wafer fab lifetime and return on investment. They will also be a fertile breeding ground for the development of breakthrough device technologies.

Combining these More than Moore devices with the memory and computing power provided by More Moore in order to create highly integrated systems lies in the domain of 'Heterogeneous Integration' - commonly referred to as System-in-Package (SiP). Heterogeneous integration extends wafer-bound 2-dimensional planarity towards 3-dimensional structures and interconnects. The main challenges are ensuring the practicality of integrating components based on widely differing technologies and materials, and introducing innovative schemes for cost-effective volume manufacturing. Together, More than Moore and Heterogeneous Integration bridge the divide between raw computing and application-specific real-world environments.

Beyond the 2015 horizon, even silicon will give way to something different when silicon-based devices reach their ultimate scaling limits. No one is quite yet sure what these 'Beyond CMOS' technologies will be, but whatever they are, they are unlikely to result in sudden transitions. Candidate technologies will almost certainly be pre-tested in the More than Moore and Heterogeneous Integration domains - the two domains where Europe is already building world-class expertise.

Enabling technologies are one thing. Designing systems that use them is another. The so-called design-gap - the difference between what can theoretically be integrated and what can practically be implemented due to design tool constraints - continues to increase. Managing this gap, by stimulating cooperation between the many different players in More Moore, More than Moore and Heterogeneous Integration to create a comprehensive 'Design Methods and Tools' domain will be a vital step in winning the system solutions race against global competition.

Putting fully engineered system solutions into production will then require equipment and materials. Europe is already a manufacturing base for some of the world's leading semiconductor materials and equipment suppliers, for whom a critical decision will be when to invest in 450-mm diameter bare wafer and 450-mm wafer handling equipment production. Equally important, they will need to meet ever-more stringent substrate purity and surface preparation requirements as the dimensions of the devices fabricated on their wafers continue to shrink. The More than Moore domain will also fuel demand for new materials and processes.

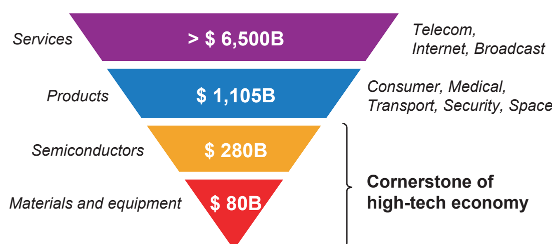
New materials and shrinking device dimensions will pose challenges for Europe's equipment makers in all aspects of semiconductor processing, from lithography and mask making through metrology and device processing to assembly and test. In parallel to 'classic' optical and EUV lithography, new mask-less lithographic techniques are emerging, such as nano-imprint and multi-beam. But despite demographic shifts in semiconductor manufacturing, Europe continues to have a strong supplier base.

All the technology domains described above have one thing in common - a growing proliferation of technology options and application opportunities resulting in an explosion in the number of materials and processes involved. However, the thread that will link them together in Europe is not fundamentally about technologies, nor is it about applications. Europe has technological know-how and market opportunity in abundance. It is about partnership in focussed R&D ecosystems where all stakeholders are stimulated to exploit their intrinsic strengths. About realising that the challenges in nanoelectronics are of such a scale that no university, no research institute, no industry player, nor even a single European country, can achieve success on its own. It's about creating a Europe-wide infrastructure for open-innovation and knowledge-sharing that recognises individual skills, that ensures people receive fair rewards for their contributions, and that looks beyond national boundaries. Such public-private partnerships require measures that equally address all stakeholders in the ecosystem in order to achieve the wider European objective - that of making the European Union the most competitive economy in the world.

Vision

Cornerstone industry

Nanoelectronics is the common denominator for an extensive suite of technologies related to silicon-based semiconductor devices. Semiconductor devices underpin the entire high-tech economy, providing a pervasive hardware platform for electronic product and service innovation in major growth markets such as automotive, avionics, consumer electronics, telecommunications, medical systems and automated manufacturing. At the beginning of the current millennium, it became possible to shrink the smallest patterns in state-of-the-art silicon-based logic devices for digital computing to below 100 nanometres. This transition from the era of microelectronics (pattern dimensions measured in microns) to the era of nanoelectronics (pattern dimensions measured in nanometres) has opened the way to totally new capabilities. To an ever-increasing extent, innovation and value creation in the growth markets mentioned above stems from nanoelectronics.



Semiconductors underpin over 16% of the global economy

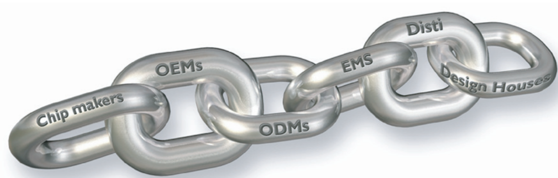
It is almost impossible to overestimate the economic value of this cornerstone industry. The worldwide market for electronic products in 2007 is estimated at $ 1105 billion, and the related electronics services market at around $ 6500 billion [1]. These product and service markets are enabled by a $ 280 billion market for semiconductor components and an associated $ 80 billion market for semiconductor equipment and materials. By comparison, the 2007 GWP (Gross World Product) is expected to reach $ 48,900 billion, implying that more than 16% of the world economy today is built on semiconductors. Figures indicate that this percentage is growing year on year. In addition to its immediate economic value, the semiconductor industry is one of the biggest investors in R&D for the knowledge society, with typical annual R&D budgets in the industry ranging from 15% to 20% of revenue. Not surprisingly, regional clusters with a high density of semiconductor industry players are also the areas with the highest rate of Intellectual Property Rights (IPR) creation [2].

Global value chain evolution

The growing complexity of nanoelectronics technology and electronic products and services in general has strongly affected the landscape of the high-tech industry. Increasing complexity results in exponential increases in capital spending and critical know-how. In the early days of semiconductors, Independent Device Makers (IDMs) could handle the entire value chain, sometimes even extending their business into manufacturing equipment and materials at one end and electronic products and services at the other. Due to extensive de-verticalisation in the industry, that model has now changed. Today, IDMs typically outsource shareable tasks to more recently established businesses such as Original Design Manufacturers (ODMs), Electronics Manufacturing Services (EMS) and Design Houses. Many successful fabless companies (semiconductor companies relying totally on third-party foundries for manufacturing) have emerged. For cost reasons, many IDMs have also entered into industrial alliances in order to jointly develop common processes.

Continuing disparity between life-cycles for technology innovation (as much as 3 years) and application innovation (as low as 6 months), increasing market demand for first-time-right and zero-defect products, and the need for semiconductor companies to provide complete hardware/software reference designs, have drastically changed the position of IDMs. No longer 'arms-length' suppliers to their customers, semiconductor companies

are now at the very heart of the innovation process in System Houses and Original Equipment Manufacturers (OEMs). As a result, the formerly linear high-tech supply chain has expanded into a series of multiple interconnected ecosystems, all of which have the semiconductor industry as an essential common element.



The semiconductor value chain has many links

In this multi-dimensional design environment where many different players are involved, it is no longer evident that an IDM's R&D and manufacturing will, can or even should be on a single site. Where and with whom a company performs the R&D related to a specific part of the value creation process is predominantly influenced by vicinity to appropriate partners (including suppliers and customers) and availability of know-how, followed by state support conditions. An early market of sufficient scale offers the potential for a higher return on investment and consequently a reduced risk. Proximity and local requirements are key factors for many of these markets and partnerships and therefore influence the choice of R&D and business location. The selection of a location for semiconductor production, on the other hand, is determined primarily by state co-investment mechanisms and by the availability of existing infrastructures.

Ecosystems for nanoelectronics innovation are evolving in various parts of the world, yet it is clear that the only ones to survive will be those in which all players (industry, academia and public authorities) cooperate with one another. Successful ecosystems must also recognise that Small and Medium size Enterprises (SMEs) and academia (universities and institutes) are fertile breeding grounds for new ideas, yet these SMEs will only thrive in the slipstream of the larger companies for whom they work [3]. This is because these larger companies are an essential gateway for expanding SME and academia generated innovation into the world economy.

For companies operating in the nanoelectronics value chain, optimised alliances and R&D involvement are critical to staying in the race. Long-term commitments, both in terms of money and people, are required from private and public stakeholders. A major part of this nanoelectronics R&D can and will be performed in Europe, because all the necessary basic competencies are already well established in Europe. This is especially true in European strongholds where close cooperation between technology development and application development is essential for success. Improving overall business conditions through effective public-private partnerships will help to strengthen and secure large parts of the value chain in Europe, thereby securing key IPR and building new skills for application leadership.

Europe 2020

On its way to 2020, Europe is already facing a number of major societal challenges. Technological solutions are foreseen for many of these challenges. Carbon dioxide emission, the major contributor to global warming, will be greatly reduced by the introduction of electric vehicles, provided of course that renewable energy sources, such as large-scale solar cells, can be adequately exploited. Transport systems in which road and car are integrated parts of a single self-controlling system will help to resolve traffic congestion. Ambient intelligence environments incorporating personal e-Health systems will limit the impact of an ageing population. Smart security systems will counter terrorist threats while still guarding personal privacy. Realizing affordable solutions for each of these challenges is an absolute necessity for Europe, and nanoelectronics is an essential enabler for those solutions.

In 2004, the European Commission (EC) published the high-level Vision2020 report [4]. This document proposes the development of a European Technology Platform (ETP) and a Strategic Research Agenda (SRA) for Nanoelectronics that will enable industry, research

organisations, universities, financial organisations, regional and Member State authorities and the EC to interact in order to provide the required resources, within a visionary program that fosters collaboration and makes best use of European talent and infrastructures. The European Nanoelectronics Initiative Advisory Council - in short ENIAC (and also the name of the world's first electronic computer) - was established to materialise the proposals in Vision2020. ENIAC's mission is to make the 2020 Information Society technologically feasible and economically affordable. The ENIAC ETP and SRA are designed as an umbrella to guide definition and execution of all R&D in nanoelectronics in Europe, including all players (industry, academia and public authorities) and all mechanisms for public-private partnerships (national, transnational, and EC) [5,6,7].

Implementation of the ENIAC SRA for nanoelectronics has clear benefits for the whole of Europe. It will provide early access to leading-edge integrated components and design skills that are essential for application in high-technology products and services. Europe's existing strengths will be reinforced in key growth markets, enabling Europe to realize its ambition of ambient intelligence - living environments that are aware of our presence and responsive to our needs [8]. Key intellectual property will be generated and benefited from in Europe, determining Europe's future shape and direction. Sufficient critical mass will be provided through large industrial players fostering SMEs and start-ups in emerging segments throughout the economic value chain. Research infrastructures will be extended, in which industry stimulates innovation-focused scientific research and education. These actions will result in the continued employment of highly skilled knowledge workers and will leverage creation of a multitude of indirect jobs. Finally, the ENIAC SRA will contribute to a sustainable economy through stimulation of energy conservation and environmental control, as well as enabling access to future alternative energy sources.

Societal needs and lead markets

Introduction

Nanoelectronics enables the development of smart electronic systems by switching, storing, receiving, and transmitting information, usually in digital form. Metaphorically speaking, this means that all smart electronic systems have the equivalent of a 'brain' for computing, plus the equivalent of 'ears, eyes, arms, and legs' to interact with the outside world. In respect to its societal relevance, the pervasive influence of nanoelectronics is closely linked to the notion of ambient intelligence as described in the 2003 study 'Science and technology roadmapping: Ambient intelligence in everyday life' led by Michael Friedewald and Olivier Da Costa [8]. Ambient intelligence is a vision of the future where the emphasis is on user-friendliness, efficient and distributed services support, user-empowerment and support for human interaction. People are surrounded by intelligent intuitive interfaces that are embedded in all kinds of objects and an environment that is capable of recognising and responding to the presence of different individuals in a seamless, unobtrusive and often invisible way. Ambient intelligence assumes a shift in computing from desktop computers to a multiplicity of computing devices in our everyday lives whereby computing moves to the background, and intelligent, ambient interfaces move into the foreground. The key words and concept are systems and technologies that are sensitive, responsive, interconnected, contextualised, transparent and intelligent.

Capturing, evaluating and integrating these qualitative factors within a systematic roadmapping process is difficult, both theoretically and practically. Instead, these qualitative 'human dimensions' have to be addressed through case-by-case studies that complement identification and characterisation of the functionalities required to address societal needs. Ordinary people do not always accept and use technology-enabled functional innovation in the way that the innovators hoped they would. In the past, there have been many market failures (for example, videotext and WAP) and unforeseen successes (such as SMS and camera phones). It is therefore difficult to accurately predict which applications will provide the trigger for achieving a critical mass of users. Moreover, people often use new technologies in ways that are very different from their intended uses - the Internet being a prime example. There is no typical, uniform user or use case, but rather a diversity of users and use-cases.

Suppliers generally have difficulty understanding the qualitative aspects of user-markets. Successful innovation is the result of a specific socio-economic and technological constellation - the right product, on the right market, at the right time - such that specific requirements in terms of user needs, user-friendliness, price, attractive supply, standards, interoperability etc. are met. If they are not, commercialisation is likely to fail. However, failed attempts may ultimately re-emerge successfully, possibly in new guises, when conditions change.

Ambient intelligence is realised into physical products and services through two main conglomerates of enabling technologies - nanoelectronics for the hardware part and embedded systems for the software part. As outlined in the previous chapter, the ETP ENIAC was installed to define and implement a strategic research agenda for nanoelectronics. In parallel, the ETP ARTEMIS was established to handle embedded systems [9]. With the growing complexity of overall systems, hardware design increasingly needs to be aided by software. In addition, flawless operation of software programs in advanced hardware circuits has become impossible without taking into account fundamental hardware parameters.

In 'Creating an Innovative Europe', the 2006 EC report by the independent expert group on R&D and innovation chaired by Esko Aho, the concept of lead markets for innovative products and services was introduced as a model for a market-oriented approach to reinforcing European research and innovation performance in the

context of the revised Lisbon Strategy [3]. Lead users, otherwise known as launching customers, in these markets are those who are prepared to take the higher initial costs and risks involved in early adoption of new innovations. They can provide important feedback to the final development of the product or service. In return, they can improve their ability to use and benefit from innovation and increase the chances that it meets their specific needs.

Because the nanoelectronics industry underlies the entire market for electronic products and services, the end customer for the vast majority of nanoelectronic technologies is the average global consumer. As a result, carving out a set of high-level societal needs in the context of ambient intelligence can provide essential guidance. Combining this guidance with known European strengths in application knowledge results in the lead market segmentation outlined in the following sections.

Health and wellness

The ageing society is a major driver for healthcare and personal wellness in Europe. Opportunities lie in e-Health, a term describing the application of Information and Communications Technologies (ICT) to a whole range of functions in the health sector. It is estimated that e-Health will account for 5% of the total EU Member States' health budget by 2010 [3]. Specific challenges include the cost of coping with an ageing population that requires prolonged medical care, and the demand for versatile, reliable systems that make patient- and therapy-specific data available to clinicians in real time. Remote patient supervision using biosensors, bio-data analysis and communication technologies are another major opportunity for cost saving.

With the advent of nanotechnology, medicine as a whole will undergo a revolution. Fast, highly sensitive DNA/protein assays made possible by innovative new bio-sensors will allow many diseases to be diagnosed 'in vitro' from simple fluid samples (blood, saliva, urine etc.) even before sufferers complain of symptoms. Similar tests will identify those pre-disposed to certain diseases, allowing them to enter screening programs that will identify early onset of the disease. Conventional and molecular imaging, increasingly combined with therapy, will pinpoint and assist in eradicating diseased tissue. Early diagnosis will lead to earlier treatment, and earlier treatment to better prognoses and after-care. By 'nipping disease in the bud' it will make many therapies either non-invasive or minimally invasive. Equipped with body-sensors that continuously monitor a patient's state of health, reporting significant changes through tele-monitoring networks, patients will be able to return home sooner and enjoy a faster recovery. Nanomedicine will also revolutionise prosthetics, with bio-implants restoring sight to the blind and hearing to the deaf. Automated drug-delivery implants will prevent conditions such as epileptic fits.

Society needs – Health and wellness

For developers of the nanoelectronic-based systems that will lie at the heart of these developments, there will be many challenges. They will, for example, need to ensure the bio-compatibility of the materials they use both for in-vitro and in-vivo applications, cope with the ultra-low power consumption requirements of wirelessly connected portable or implantable systems, and stay within the maximum thermal loads that implanted devices can impose on the human body. In many cases, biosensors will have to achieve phenomenal sensitivities, equivalent to detecting the presence of a grain of salt in an Olympic swimming pool. Developing implants in bio-compatible packages will push miniaturisation to the limits, while at the same time requiring the integration of many different types of device - for example, bio-

sensors, nanoscale MEMS (microelectromechanical systems) devices, optical components, energy scavenging systems and RF (radiofrequency) interfaces. Many of these highly complex heterogeneous systems will also need to achieve life-support system reliability.

Transport and mobility

Mobility and safety are clear societal needs for the future intelligent road. The European transport system is a vital element in ensuring Europe's economic and social prosperity. It serves key roles in the transportation of people and goods in a local, regional, national, European and international context. An integrated approach that links all modes of transport (air, rail, road and waterway), addresses the socio-economic and technological dimensions of research and knowledge development, and encapsulates both innovation and the policy framework is essential for ensuring that sustainable and competitive transport solutions make a visible and positive difference for Europe, its citizens and its industry.

Society needs – Transport and mobility

As the volume of traffic on our roads continues to increase, there will be an increased demand for safe drive-by-wire systems that out-perform humans in terms of speed control and collision avoidance. At the same time there will be a need to transfer much more information to and from moving vehicles, not only for driver information, navigation and entertainment, but also for vehicle tracking and road toll applications. Ultimately, this will extend to road intelligence systems for real-time interaction between vehicles with their environment. The world's limited oil and energy resources will stimulate the development of far more fuel-efficient vehicles as well as new alternative energy (battery or fuel-cell powered) vehicles. Nanoelectronics will be at the heart of many of these advances.

Electronic systems for automotive applications have to withstand very harsh environments, including high temperatures, humidity, vibration, fluid contamination and electro-magnetic compatibility. While these problems have largely been solved for conventional integrated circuit (IC) style packaged devices, a whole new set of challenges will have to be faced when these packages also contain integrated sensors, actuators, mechatronics or opto-electronic functions. Some systems, such as collision avoidance radars and engine-assist/traction motor drives, will push the performance limits of current high-volume low-cost semiconductor solutions in terms of frequency capability and/or power/thermal handling. In addition, the safety-critical nature of drive-by-wire systems will require extreme reliability, measured in parts per billion instead of today's parts per million. Similarly, other transportation systems in Europe, such as aircraft and trains, will need advanced electronic solutions in which nanoelectronics can play a differentiating role.

Security and safety

Statistics show that we live in a much safer world, yet there is still constant demand for increased safety and security in virtually every aspect of our lives, driven by the principle that 'one death is one death too many'. It reflects itself in public demand for personal emergency and home security systems, and government led protection from crime and terrorism. However, this is always accompanied by the need for personal protection without restriction of liberty or limitation of privacy, which means that safety and security systems need to be reliable, easy to use and capable of safeguarding the privacy of end users. It is in this area that ambient intelligence's ability to recognise individuals and be responsive to their individual needs will be highly valuable. Nanoelectronics will provide the necessary sensors, computing power and reliability at cost levels that allow

safety and security to be built into the fabric of our environment.

Society needs – Security and safety

Safety and security systems can be divided into two groups. Firstly, low-cost personal emergency and home protection systems that are affordable for consumers. Secondly, high-performance high-efficiency systems for applications such as banking, passports and other identification cards, public transportation, telecommunications and other safety critical systems. Together, the systems in this second group outline the rapidly growing e-Government market in which smart cards and RF-ID are the most evident components.

It is clear that safety and security not only constitute a major market in themselves. They are also generic enablers for many other applications. To make these systems unobtrusive enough so that we do not end up resenting them, they must be small, robust, and easy to use. This puts high demands on miniaturisation and low power consumption. Yet their requirement to be highly reliable also means that they must be complex and multi-functional, so that they make decisions based not on a single parameter but on combinations of parameters (e.g. fingerprint, voice, iris pattern). This will involve the integration of a wide range of sensors, MEMS and opto-electronic devices. Such devices will also need to communicate reliably by wired and wireless networks, and they must be made tamper proof and able to withstand environmental conditions that might affect their performance (e.g. radiation, chemical corrosion, shock).

Energy and environment

Environmental technologies and eco-innovation industries in the EU account for about one-third of the global market. Overall, the sector has enjoyed significant growth over the past decade. In addition to being an area of significant technological opportunity and importance for people's quality of life, this sector is amenable to promotion through measures complementary to R&D, such as the promotion of energy efficiency, the adoption of green public procurement policies and economic instruments such as taxation. The range of technologies encompassed is very large, including new energy efficiency and energy generation technologies as well as conservation, recycling, waste reduction, emissions control and environmental control. Environmental considerations are also central to most other sectors including construction, transport and agriculture. Consequently, it will be necessary to find a focus for large-scale strategic actions.

Equally important are the environmental aspects of many of the lead markets for nanoelectronics mentioned earlier. Energy efficiency and low-power operation are innovation drivers in virtually all electronic circuits designed today. Solid-state lighting is a clear example of an emerging market where nanoelectronics and energy saving go hand in hand. Environmental monitoring and control, using smart sensor networks, is also a potentially high-volume market.

Society needs – Energy and environment

However, the biggest impact of nanoelectronics will be in enabling the introduction of new and CO_2-free energy sources, such as highly efficient solar energy conversion and hydrogen fuel (the basis of the so-called hydrogen economy), and the development of electric transportation to replace vehicles driven by internal combustion engines. Nanoelectronics will enable the energy management systems needed to utilise these new and diversified energy sources. It is estimated that by the end of the 21st century, at least 70% of the world's energy requirements will need to be fulfilled through these new sources, as most sources in existence today will either be exhausted or unacceptable because of their detrimental effect on global warming [1]. While many of the building blocks needed to utilise these new energy sources are considered technically feasible today, they will not become affordable without nanoelectronics-enabled innovations.

As portable communications devices pack more functionality, low-power consumption will become an even more critical requirement. The need to keep devices active for long periods of time between battery recharges, or even to make them autonomous in terms of energy supply, will require the integration of energy scavenging devices that pull and store power from the local environment. At the same time, affordability, reliability and environmental compatibility (disposability, recycling and re-use) will be other major drivers. It should also be recognised that the pervasiveness of wireless systems is possible only through the huge underlying infrastructure of wired channels in homes and in the public domain. These data transmission functions need to be continuously upgraded by implementing high-volume, low-cost nanoelectronic devices.

Communication

People are becoming used to having easy access to friends, family and information services and more frustrated when that access is not available to them. Making information available anywhere at any time relies on connectivity and communications, increasingly via the use of wireless-based networks (e.g. cell phones, Wi-Fi networks) to meet the 'anywhere' requirement. In future, communication systems must be even easier to use than they are today, even to the point where specific connectivity channels become irrelevant to the user. Information will simply tunnel itself to its destination by whatever communications channels are available. At the same time, the bandwidth of communication systems will have to increase dramatically in order to cope with the increasing amount of data that people will want to move around (e.g. voice, pictures, video, file transfer) and they will need to become much more secure against eavesdroppers and hackers.

Society needs - Communication

In common with security, communications is a common factor driving functionality for a broad and still expanding portfolio of products and services. Nanoelectronics will be needed not only to meet the miniaturisation and low-power requirements of handheld portable communications devices. It will also be needed to allow much more functionality, in terms of the number of different communication channels, to be packed inside them. The 'multi-band multi-mode' devices that this enables will be the key to decoupling communication from specific communication pipes, heralding a whole new era of seamless communications. At the same time, wireless communications channels will move to higher frequencies in order to increase data rates and maximise spectrum usage. This will require ever-greater integration of RF interfaces and the development of new RF architectures that allow circuitry to be re-used across many different RF channels and modulation schemes.

As portable communications devices pack more functionality, low-power consumption will become an even more critical requirement. The need to keep devices active for long periods of time between battery recharges, or even to make them autonomous in terms of energy supply, will require the integration of energy scavenging devices that pull and store power from the local environment. At the same time, affordability, reliability and environmental compatibility (disposability, recycling and re-use) will be other major drivers. It should also be recognised that the pervasiveness of wireless systems is possible only through the huge underlying infrastructure of wired channels in homes and in the public domain. These data transmission functions need to be continuously upgraded by implementing high-volume, low-cost nanoelectronic devices.

Infotainment

The creative industries provide a strong cultural component to the European economy, in sectors such as broadcasting, film, Internet, mobile content, music, printed media, electronic publishing, video and computer games. This sector, for which Europe's strong cultural heritage provides a sound basis, is important for innovation in two ways. Firstly, it increasingly leverages the new media technologies associated with the digital revolution. These disruptive technologies, which include digital coding and distributed content generation, processing, sharing and recording, are significantly changing the value chain in this industry. The convergence of shared technologies and markets (for example, the camera-phone plus MP3 player plus TV on mobile), the protection of intellectual property rights and the emergence of new distribution channels are all key factors. Given the global reach and borderless nature of the network environment, a review is called for in respect of the territorial aspects of the copyright system and of appropriate frameworks for efficient licensing of copyrighted content across national borders. Secondly, R&D is itself increasingly seen as a creative industry that flourishes in a creative economy, because it draws together in intimate and powerful combinations the spheres of innovation (technological creativity), business (economic creativity) and culture (artistic and cultural creativity). The combination of content and technology is increasingly seen as a core feature of regions that are attractive to entrepreneurs.

Content must not only be accessible anywhere and anytime. It must also be of the right quality and accessible in the right format to fulfil user needs in ambient intelligence environments. Access to similar information will be required in many different locations (e.g. home, car, street, hotel) and delivered through a variety of channels (terrestrial, satellite, cable, phone line, wireless, discs). Yet in each location the rendering device for that content, and people's expectations of it, will be different (for example, what is expected from a flat-panel TV set compared to what is expected from a video-phone). Digital media, such as DVDs and HDTV, have increased people's expectations of video quality, yet this video quality will often have to be delivered through existing networks.

Society needs - Infotainment

The need to deliver high quality media through a range of different communications channels while maintaining the required quality will require new developments in multi-format encoder/decoders, data compression and transmission systems. Media senders (for example, Internet servers) will need to automatically tailor transmission to suit the capabilities of the rendering device on which the content will be experienced. Storage and distribution (CD, DVD, digital home networks) will need to be developed that are compatible with the digital

rights management requirements of content providers. Content generators will require new equipment (for example, HDTV studio equipment and lightweight portable HDTV cameras) to capture content and content providers will need advanced video compression and transmission schemes to distribute it. The demand for users to create their own content will also require significant advances in areas such as image capture (digital cameras, camcorders), image analysis and picture quality improvement at affordable consumer-product prices.

Conclusion

The above sections provide a skeleton for translating societal needs into future applications and lead markets that satisfy those needs, with visionary examples of the intelligent systems that are expected to emerge in each of these markets. From a historical point of view, it is possible to see three extended waves of evolution in electronics-enabled application development. The first wave, roughly positioned from 1965 to 1985, was the period during which people were barely touched by consumer products created by means of microelectronics. This was the time of multi-channel TV broadcasting, videocassette recorders and mainframe computers. The second wave, between 1985 and 2005, saw the explosive growth of CD and DVD, personal computing and gaming, mobile telephony, and global proliferation of the worldwide web. In hindsight, however, it is evident that this second wave was only the tip of the iceberg. The third wave, enabled by the shift from microelectronics to nanoelectronics has just begun. This new wave, which may last until 2025, will see the development of true ambient intelligence systems everywhere, with nanoelectronics penetrating all aspects of everyday life, from the personal (domotics, lifestyle, wellness, health) to the public (energy, mass transport, buildings).

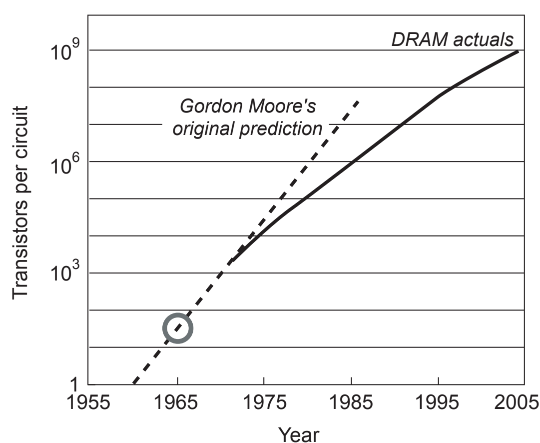
Unfortunately, the high-tech economy is complicated by the fact that it is hard to predict exactly what new products will emerge in volume and when. Although ambient intelligence does provide a guiding vision, specific extrapolation from application roadmaps into tangible products is not straightforward and, to an extent, not even feasible. As a consequence, the nanoelectronics industry as a whole is still largely technology-driven, creating multiple opportunities for end markets in which consumers eventually decide. An inevitable consequence of this approach is that relative R&D spending cannot stabilise - as is needed in the present environment of business consolidation - but continues to increase. A concern for the entire sector is that overall R&D spending may in fact decline and that emerging and interesting new opportunities will not be identified and matured in time. This asymmetry between research costs and market returns is a serious risk.

However, it is still possible to extrapolate from observed trends in high-level system parameters. Relevant key parameters are computing power, data storage, communication bandwidth and data rate, which are all increasing, and the energy dissipation per bit or per circuit element, which is decreasing. Such trends are usually expressed as an increase in performance over time at fixed costs, and most of them have changed exponentially over the last two decades. Solid-state data storage capacity and computing power, for example, have increased by a factor of 10 over the past 8 years. To continue this rapid progress in technical capabilities is one of the most critical areas for realizing the vision of ambient intelligence, for example, in safe driving for automotive, data compression and channel compensation in communication, and voice and face recognition in security. In the Technology Domains sections of this Strategic Research Agenda, these trends are extended and connected to the underlying roadmaps for nanoelectronics technology innovation.

Technology domains

Introduction

The origin of nanoelectronics innovation can be traced back to two events that occurred in 1959. One is Richard Feynman's talk 'There's Plenty of Room at the Bottom' in which Feynman shared the insight that many seemingly impossible questions on miniaturisation can be answered from realising that the Laws of Physics do not forbid it [10]. The other is Jack Kilby's patent submission 'Miniaturised Electronic Circuits' on making resistors and capacitors together with transistors on one and the same silicon substrate, a concept we know today as the integrated circuit or silicon chip. Just a few years after these events, Gordon Moore stated a bold extrapolation from observed market trends in which he inferred that the cost of delivering digital functions on silicon wafers - for example, the storing of one bit of information - can be halved every one or two years for a considerable time to come [11]. This bold cost-down prediction of exponential growth turned out to be largely correct and over the years became known as Moore's Law. Moore's Law is not a law of nature but an economic argument reflecting a careful balance between the cost of innovation and the benefits of growth in the electronics industry. It has allowed the electronics industry to grow to its current pervasive presence in all aspects of society.



Moore's Law is about more digital logic for the same price

The ability to combine an exponentially increasing number of functions on one IC without increasing its cost has caused a physical size implosion of all systems that require large amounts of electronic circuitry. Constructed from discrete components, early computers would easily fill multiple filing cabinets, but with advances in integration soon collapsed to the size of a single drawer, then to a single board, and eventually to a single silicon chip. As a result, computing became affordable for non-military applications, then for individual office workers, and eventually for consumers. In quantitative terms, Jack Kilby's single-switch invention way back in 1959 eventually evolved into silicon chips that today can easily carry as much switching elements (transistors) as there are people on Planet Earth.

With exponential expansion in system and circuit complexity, it was not only overall performance that went up with it. The associated technological challenges also grew dramatically. Although nanoelectronics has only recently entered the nanotechnology domain (pattern dimensions below 100 nanometres), it has evolved far beyond its humble origins in the fabrication of transistors on silicon wafers. Identifying and predicting the key parameters and main technical challenges in the industry has become a business in itself through the International Technology Roadmap for Semiconductors (ITRS) [12]. Today, the ITRS is a global forum populated by semiconductor manufacturers, equipment and material suppliers, institutes and universities. The information provided in its annual symposia plays a leading role in determining the world's semiconductor innovation agenda.

In order to be able to draw clear roadmaps and assign tangible research priorities, structuring R&D into technology domains is needed in parallel with the application domains described earlier. The technology domains introduced in this SRA are derived from their place in the industrial ecosystem. This approach eases interaction between the players involved by providing a common ground and vocabulary for each domain.

Together, the domains cover the nanoelectronic landscape in Europe. Where appropriate, reference is made to the ITRS in its role as the global binding factor between the industrial and academic semiconductor communities.

Domain 'More Moore'

Rationale

The 'More Moore' domain is internationally defined as an attempt to further develop advanced CMOS technologies and reduce the associated cost per function along two axes. The first of these axes is a geometrical (constant field) scaling, which refers to the continued shrinking of horizontal and vertical physical feature sizes of on-chip logic and memory storage functions in order to improve integration density (reduced cost per function), performance (higher speed, lower power) and reliability values. The second axis of scaling relates to 3-dimensional device structure ('Design Factor') improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip. This axis of 'equivalent' scaling occurs in conjunction with, and also enables, continued geometrical scaling.

Almost 70% of the total semiconductor components market is directly impacted by advanced CMOS miniaturization achieved in the More Moore domain. This 70% comprises three component groups of similar size, namely microprocessors, mass memories, and digital logic. The analog / mixed-signal market largely relies on variants of CMOS technology that are less affected by the miniaturization race due to other constraints, such as the need to handle power and/or high voltage. Moore's Law generates a technical challenge for engineers but at the same time is auto fed by the productivity gain that it brings. It is this economic aspect of Moore's Law that has made electronics so pervasive. Over a period of 25 years, the semiconductor industry has achieved a 30,000-fold increase in the number of transistors that can be produced on a square cm of silicon, while the average price of each transistor has been reduced by a factor of 2500.

Thanks to collaborative projects supported by public authorities and European programs, as well as R&D alliances, Europe has caught up over the last 15 years to the point where its CMOS technological expertise is now on a par with the rest of the world. European IDMs have stayed competitive in the memory market by spinning out their memory activities into separate companies that nevertheless maintain their strong European roots. Today, these companies are world leaders in Dynamic Random Access Memory (DRAM) and NOR Flash Non-Volatile Memory (NVM). Europe has also attracted large-scale foreign investment in the form of European-based manufacturing plants for the world's two largest microprocessor companies. Europe is also home to the world leader in advanced lithography equipment. As a result, there is still a strong interest for Europe to pursue research in the 'More Moore' domain. In the digital logic segment, however, manufacturing is becoming increasingly difficult for independent IDMs because their addressable markets no longer allow them to achieve the required economy of scale. Since the mid 1990's, there has been a trend towards fabless and foundry models for virtually all logic products other than microprocessors and memories. Foundries deliver advanced, yet generic, digital CMOS technology platforms to design houses and are now at the forefront of the Moore's Law battle. Where IDMs have existing manufacturing lines, they typically employ them to concentrate on areas other than pure digital CMOS (value-added technology options and/or 'More Than Moore' technologies). Although these diversified technologies lag behind introduction of the CMOS processes on which they are based, they nevertheless benefit from progress in CMOS research and the associated know-how in lithography and other related techniques.

To stay in business, IDMs producing digital logic products must therefore maintain access to leading-edge core CMOS technologies in order to develop value-added options/derivatives, as well as to master the associated manufacturing science. Fabless and fab-lite companies will therefore still need to be heavily involved in 'More Moore' R&D and they will still need to find well-trained technology, device and circuit experts from research institutes and academia. For IDMs, remaining

state-of-the-art in 'More Moore' technologies is also the best way to become a participant in the 'Beyond CMOS' era, because the transition is more likely to be a gradual one rather than a totally disruptive one.

As CMOS nears its ultimate limits, the cost of R&D will continue to escalate and R&D consortia/alliances will need to become financially stronger in order to cope. Only a few such consortia/alliances with the necessary resources exist in the world today. To remain on course, Europe has no choice but to extend collaboration and cooperation between all players in the R&D and production value chains, either horizontally (between competitors) or vertically. If Europe cannot find enough players (or players with sufficient resources) in certain areas, it must engage in overseas collaboration/cooperation in order to achieve critical mass. Vibrant 'More Moore' research in Europe will guaranty a stronger position for European players in such global consortia. Private-public partnership has been the foundation for the collaboration activities over the past years. It must be continuously re-evaluated in order to maintain the level of resources in line with escalating technical complexity and competition.

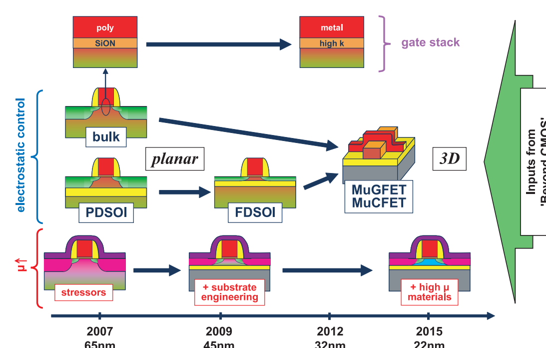
Research Priorities

In 1965, manufacturing relied on 25-mm diameter wafers. Today it's done on 300 mm wafers. Over the same period, the smallest patterns on these wafers have been reduced from 6 - 8 microns to around 20 nanometres. This, in a nutshell, is what More Moore is about. On the way, the internationally accepted ITRS roadmap has and continues to set the pace, identifying the new 'technology generations' that will be introduced every 2 to 3 years and highlighting an increasing number of technical challenges that must be addressed. In addition to geometrical scaling, material and architecture innovations will play a more important role in the future to enable further increases in device performance. It is not the intent of this section to duplicate the ITRS, but rather to outline the priorities from a European perspective.

Digital logic

Although continuous reduction in the size of CMOS transistors (the basic building block of logic circuits) has delivered enhanced performance for decades in terms of speed, power consumption, reliability and cost per function, further progress is needed to tackle more complex optimisations. At the same time, the diversity of the options that need exploring is also an opportunity for innovation and a challenge.

As the critical dimensions of CMOS transistors are scaled down, leakage currents and the associated static power consumption become a major issue. Ultra-thin Silicon OxyNitride (SiON) gate dielectric suffers from a significant tunnel leakage current and alternative materials such as 'high-k' dielectrics are therefore being brought to production-worthy maturity. Their physical and electrical properties are intensively studied by academia, as is their ability to be integrated into the processing sequence. Hafnium compounds will be used starting at the 45-nm node.



Advanced CMOS transistor architecture roadmap

High-k dielectrics and the control of low threshold voltages make it necessary to replace traditional polysilicon gate electrodes by metal electrodes, with different metals possibly being required for the gates of n- and p-channel devices. New source/drain architectures such as low Schottky barrier would be useful to enhance current capability. At the same time, the electrostatic control of the gate is more challenging at low critical dimensions and the variability of the transistor characteristics at high doping level may alter the functionality of logic gates as feature sizes are scaled down. This means that more sophisticated transistor architectures using three-dimensional structures, such as multiple-gate FETs (MuGFETs) or multiple-channel FETs

(MuCFETs), will be needed in the future. However, the process complexity needed to fabricate these devices has so far prevented their early introduction into manufacturing. The 22-nm node will probably be the entry point for these disruptive technologies.
When it comes to enhancing speed, many options are already approaching maturity. In the shorter term, it is being achieved by inducing stress in the conductive channel of the transistor and/or by using different crystal orientations. In the longer term, it may be achieved by replacing silicon channels with more conductive materials such as Germanium (Ge) or III-V compounds embedded in more sophisticated architectures (e.g. GeOI, III-V on Ge, nanowires).

Gradual integration of these innovations into manufacturing, together with co-design of engineered substrates, material stacks and devices, will enhance the present bulk or SOI planar transistor, allowing a steady increase in overall performance. These innovations provide a technical pathway to having the 16-nm node in production by 2015. Increasing attention is needed for the modelling of phonon propagation, since confined acoustic phonons can limit mobility in SOI substrates, and phonon quantisation leads to reduced thermal conduction in future low-k materials. The increasing statistical variability introduced by the fundamental discreetness of charge and the granularity of matter needs special attention, better understanding, modelling and monitoring. It will trigger fundamental changes in the way circuit and systems are designed in the future.

Although transistor performance will continue to increase, the performance of the interconnects between the transistors is not expected to keep pace. The effective resistivity of copper interconnects increases at small dimensions and the dielectric constant of the insulating film below and between the interconnect layers does not scale much (even with so-called 'low-k' dielectric materials). As a result, signal integrity in the connections is becoming a major issue. Strong cooperation between the technology and design communities will be needed to overcome the future limitations of Cu/low-k interconnects. Long-term innovations such as self-assembled nanoporous dielectrics with enhanced structural strength, air-gap dielectrics and 3D interconnects will require major development work, while disruptive concepts are unlikely to totally replace the Cu/low-k stack. Carbon nanotubes and silicon nanowires are alternatives under study.

Europe is well positioned to handle the challenge of advanced logic processes. It has leading applied research institutes driving the development of new semiconductor devices and new front-end and back-end processes. It has strong academic expertise in specialized areas, especially in materials, TCAD, and electrical and structural characterization. Provided there is greater efficiency in the link between academia and industrial research, it is possible that the multicultural expertise, diversity of approaches and cooperation between R&D teams in Europe will be key assets in maintaining Europe's worldwide competitiveness in innovation.

Priorities until 2013

- Develop technology and devices for high-k / metal-gate stacks for 45-nm and 32-nm generations
- Develop technology and device architectures for multi-gate and multi-channel devices for 32-nm or 22-nm generations
- Assess the limits of the low-k/ Cu intercon nect scheme and develop innovative solutions (air gap, 3D interconnects)
- Develop co-engineered substrates - high mobility materials - to enable the 16-nm node.
- Develop a physical understanding of the limits of transistors, e.g. transport physical mechanisms, device matching, impact of atomic-level statistical fluctuations, reliability limitations.
- Foster a strong link between device design technology, simulation and circuit & system design
- Allow timely development of adaptively optimized Design for Manufacturing (DFM).

Priorities from 2013 to 2020

- Develop a physical understanding of the funda men tal limits of ultimate CMOS transistors structures, e.g. quantum effects transport physical mechanism, impact of atomic-level statistical variability, reliability limitations.

- Prepare the co-integration of CMOS with novel 'Beyond CMOS' structures.

Memories

Memories often consume most of the silicon area in complex ICs. The driving parameters for advanced memories are primarily integration density (achieved through aggressive scaling), followed by non-volatility, speed and energy consumption. As stand-alone devices, memories are in the midst of an intensely competitive battle between manufacturers, with selling prices falling rapidly soon after the introduction of new memory densities. This has resulted in significant consolidation, and market conditions that favour pure-play memory manufacturers. IDMs concentrate on embedded DRAM and/or embedded NVM as options that can be added onto core CMOS technology.

DRAM

Stand-alone or embedded in ICs, DRAM targets very high storage capacity together with reasonable data retention. Scaling device dimensions in order to increase storage density translates into very demanding lithography, extremely high aspect-ratios that push deposition and etching to their limits, new materials for the capacitors and ultra low-leakage access transistors. This last factor is the main driver behind the development of 3D transistor structures such as FinFETs for introduction one generation in advance of that for logic devices. The question is whether or not the increasing process complexity will reduce the productivity gain expected from pure scaling (30% bit cost reduction per year). This is why the introduction of 450-mm diameter wafers will be required in the longer term, provided that the cost of equipment development can be overcome by the industry.

Europe has a strong development and manufacturing base and can rely on the flexibility of R&D institutes to develop and integrate new materials. Integration of new materials will especially be needed for the DRAM capacitor, where reliable high-k dielectrics with low equivalent thickness will be needed, and where the transition from a Metal-Insulator-Semiconductor (MIS) to a Metal-Insulator-Metal (MIM) capacitor is expected at the 45-nm generation.

DRAM priorities

- Development of new materials for DRAM capacitors
- Develop new memory structures for beyond 30-nm (e.g. interleaved capacitor DRAM)
- Introduction of 450-mm wafers (see E&M section)

Non-Volatile Memory (NVM)

NVM is an important feature in many products and the current mainstream technology for implementing it is Flash (NAND or NOR type), both for stand-alone NVM devices for mass storage and NVM embedded in SoCs. Europe has strong research centres and universities with good expertise in NVM and the European semiconductor industry is also strongly involved in NVM products. However, non-European companies drive technology leadership in NVM, particularly in NAND Flash.

From a technology perspective, scaling current Flash processes will be the preferred route for as long as the introduction of new materials and architectures does not become mandatory. High-k materials are expected to be introduced firstly as an inter-poly dielectric at the 32-nm node, while a crested barrier could replace the tunnel oxide at the 22-nm node. Coupling between cells is a major issue in NAND Flash memory arrays and will push the introduction of low-k dielectric from the 45-nm node onwards. Later on, probably at the 22-nm node, both NAND and NOR Flash will require three-dimensional cell structures. Nanoparticle storage emerging from nanotechnology developments may find some applications, provided that a clear path exists for further downscaling.

Emerging 'unified' memories with the performance of SRAM and the density of DRAM, together with non-volatility, are the object of a continuous quest. Some concepts such as Ferro-Electric RAM (FeRAM) are already in production, while others such as Magnetic RAM (MRAM) are starting. However, with all of these technologies scaling to smaller geometries seems to be problematic in the long term. In this respect, Phase-Change RAM (PCRAM) using chalcogenide offers more promise. In addition, the introduction of inherently bi-stable materials (bi-stable at the molecular level) as the base element for high-density unified memories is still

at the 'proof of concept' stage. For these approaches, research is needed both in terms of material science and architecture exploration in order to demonstrate their potential to surpass the expected performance of scaled Flash devices.

NVM priorities until 2013

- New materials: high-k as interpoly dielectric, discrete traps layer for charge storage, low-k
- 3D cell structure exploration
- Research on new concept / materials, new memory cell / array architectures

NVM priorities from 2013 to 2020

- Unified memories competitive with scaled flash memories (e.g. cell size, reliability, CMOS com patibility, scalability)

Cross-cutting issues

'Low power' is a key requirement in More Moore, especially for the types of product developed in Europe. In most cases, it is unreasonable to expect breakthroughs from a pure technology standpoint or from a pure design methodology. Enhanced synergy between application, design, device and process development will be a key asset for those organizations attempting to find an efficient way to achieve low-power systems.

Making ever-shrinking patterns on full wafers in a production environment is probably the most visible physical feature of the More Moore domain. More Moore leans heavily on the Lithography segment of the 'Equipment and Materials' domain to make this possible. Europe has a major lead in this field through dominant suppliers, research institutes and advanced pilot lines.
In addition to the need for tightened specifications for lithographic tools and materials, stronger interaction is needed between designers, process engineers and providers of design tools in order to relax the lithographic constraint of printing features 'as-designed' onto the wafer. Research work into Design for Manufacturability as explained in the domain 'Design Methods and Tools' should provide ways of tackling the problem of escalating mask costs, for example, by applying Optical Proximity Correction (OPC) only to functionally critical patterns or by the generation of more regular layouts. It should also be stressed that OPC impacts significantly the variability and yield of circuits calling for this reinforced synergy between design and technology. A scientific understanding of process steps (e.g. clean, etch, Chemical Mechanical Polishing (CMP), etc.) is needed to complement the pragmatic approach of process engineering, especially as we enter the nanometre regime.

The development of structural in-line metrology (accurate 3D measurement of different patterns, overlays etc.), fast and sensitive defect detection and classification, structural off-line characterization (including morphological, physical and chemical analysis of 3D nm-sized structures made of complex material stacks), and methods of assessing the sources of process variability, is a challenging research field which may boost or hinder technological developments. It should be stressed that Europe has key expertise and major infrastructures (e.g. a synchrotron) to address the challenge.

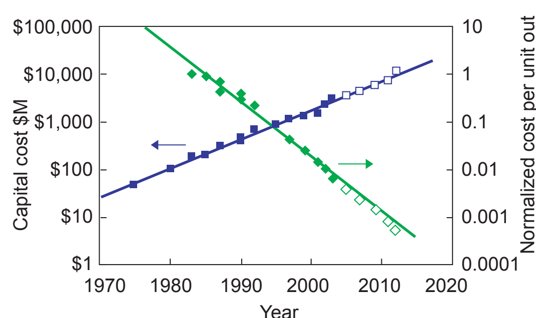
A physical understanding of the morphological and electrical behaviour of all functional structures (including dispersion, yield and reliability issues), the development of accurate physical models (including TCAD tools) and their abstraction into accurate compact models are mandatory for designing complex circuits. Many cooperative programs and the strong commitment of a few leading institutes have brought European TCAD expertise to the highest level. Compact models developed in Europe have been recognized as international standards. Strong support is needed to maintain this leadership for future technologies.

Being competitive in running state-of-the-art advanced volume manufacturing wafer fabs with a typical investment of € 3 billion requires state-of-the-art knowledge in a large number of production related areas. These include optimisation of resources (energy, water, silicon, gases), automation of equipment, robotics, software for computer-aided manufacturing, shop floor scheduling, yield enhancement techniques (defect control, advanced process control, advanced equipment control, design of experiment, engineering data analysis), to name but a

few. The possible transition to newer factories using 450-mm wafers with total automation will also be an active field of development that needs to be started very soon.

Implementation

During the course of FP7, advanced CMOS technology miniaturization will continue, even though increasing difficulties may slow down pure technological progress. The More Moore domain is the one that requires the largest effort in R&D related to processes, semiconductor technology integration and circuit design as well as equipment and materials - see domain 'Equipment and Materials' - while integrating inputs from the 'Beyond CMOS' domain as time progresses. Delivering leading nanoelectronic technologies, enabled by new materials, device concepts and circuit paradigms, to customers requires investments in manufacturing plants in excess of € 3 Billion, implying that mastering the manufacturing science will play a pivotal role in ensuring competitiveness. This trend calls for increased involvement by the academic community in the design, technology and manufacturing ecosystem, because a high degree of innovation and a better fundamental understanding of complex phenomena are needed. At the same time, education should promote the fact that real science and real breakthroughs exist in a domain where manufacturing is central to progress.



Advanced CMOS wafer fab cost trend

Europe has good potential to bring solutions to the technical challenges in the More Moore domain to ensure steady progress. As its technical focus, Europe should maintain its leadership in lithography, reinforce its materials research oriented towards nanoelectronics, promote synergy between technology, design and application domains, and maintain its excellence in specific areas such as compact models, TCAD and IP generation.

However, in order to reinforce the efficiency of the whole R&D supply chain from academia to applied research institutes and industry, many specific facts from the More Moore domain need to be highlighted. Most R&D is driven by the industry, especially through the ITRS, because much of it is short to medium-term oriented. The introduction of new materials together with inevitable atomic-scale variability and the need for an in-depth understanding and modelling of the complex behaviour of deeply scaled devices will increase the role of academia in the More Moore domain. Final process integration is cost and capital intensive. It can be done only in state-of-the-art facilities that act both as a lab and as a fab, lowering overall equipment depreciation costs and ensuring a seamless technology transfer to manufacturing. This is because there is a strong interaction between the equipment used and the final (electrical, reliability, yield, variability) performance that can be achieved. R&D using 300-mm silicon wafers is beyond the financial capacity of individual organizations or countries. It needs strong support at the European level to complement national and/or industrial initiatives. For early technology assessment, there is a need for flexible low-cost lines combined with strong scientific expertise, which can be achieved at the national level and networked at the European level. Manufacturing awareness on the part of researchers is definitely needed in order to focus their work on fields that have the potential for introduction into volume production lines.

Taking these facts into account, we recommend that future R&D support programs in Europe:

- Focus funding on one or two state-of-the-art 300-mm research infrastructures capable of full process implementation, linked with a network of smaller, lighter, flexible infrastructures for exploratory research;
- Give guidance and stimulate networks of academic excellence that have access to these infrastructures;
- Enable the establishment of cooperations with leading research organizations outside Europe;

- Support long-term collaborative projects between industry and academia, along the lines of a jointly defined vision established with industry guidance and targeted at creating excellence in European nanoelectronics research;
- Boost support to projects aiming at enhanced inter action between technology and circuit/system design, addressing the challenges of designing billions of transistors for complex Systems-on-Chip (SoC);
- Encourage academia and industry to make nanoelec tronics more attractive to talented young people in both the technology R&D and manufacturing science areas.

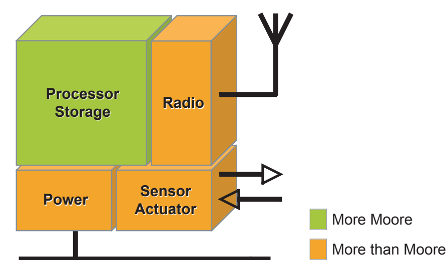
Domain 'More than Moore'

Rationale

From a technology perspective, 'More than Moore' (MtM) refers to a set of technologies that enable non-digital micro/nanoelectronic functions. They are based on, or derived from, silicon technology but do not necessarily scale with Moore's Law. From the application perspective, MtM enables functions equivalent to eyes, ears, arms and legs, that allow the world of digital computing and data storage (the brains) to interact with the real world. MtM devices typically provide conversion of non-digital as well as non-electronic information, such as mechanical, thermal, acoustic, chemical, optical and biomedical functions, to digital data and visa versa. Clearly MtM technologies and products provide essential functional enrichment to the digital CMOS based mainstream semiconductors. Together with conventional IC technology (More Moore), MtM has become one of the major innovation drivers for a very broad spectrum of societally relevant applications. The emerging and rapid development of MtM technologies and products is mainly driven by three factors.

The need for functionality beyond digital computing in order to interface to the real world in a wide range of societally relevant applications. Intelligent systems need not only memory and processor, but also power, RF interfaces for wired and wireless communication, and sense and actuator functions. With industry entering into the nanoelectronics era, more and more consumers demand more functionalities beside the digital one. A modern mobile phone is a good example of an electronic product with a significant number of non-digital functions - radio-frequency voice communications, audio/video player, camera etc.. The transport sector also includes many applications where a large number of sensors and actuators are required - for example, engine control, safety, navigation and comfort systems

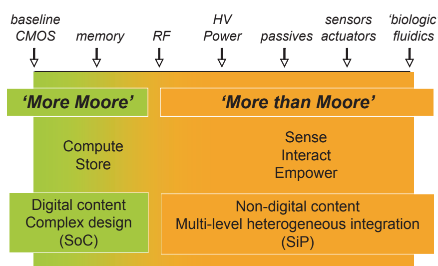
The need to create innovative products and broaden the product portfolio manufacturability using existing wafer technology and production lines. Due to fierce competition and high investment costs, it is not easy to ensure business profitability by producing commodity ICs. MtM products can add value on top of commodity CMOS technology and product portfolios. MtM technology will not only help to enlarge existing markets. It will also drive the development of emerging ones. MtM is a unique opportunity for creativity, innovation and new business creation for both small and large companies.



Intelligent systems need a Brain, but they also need Ears, Eyes, Arms and Legs

The need to master the design of heterogeneous systems that combine digital and non-digital functions. Current System-on-Chip (SoC) design methodologies primarily target the rapid reliable design of large complex digital chips. Even though many non-digital functions can theoretically be integrated onto these chips, doing so would involve prohibitive development time and cost. In addition, there is little prospect of a single practical technology that would allow such integration in the near future. It is therefore of paramount importance to develop design methodologies that balance the

benefits of integrating some MtM functions on a chip, while integrating others in the same package to create System-in-Package (SiP) solutions.



More Moore and More than Moore are complementary

Research priorities

Radio frequency (RF)

Many of today's electronic systems use RF circuits to transmit data internally or externally. Typical RF applications include mobile wireless communications (e.g. cell phones), wired communication (e.g. broadband Internet) and short-range connectivity (e.g. Bluetooth). Mobile RF applications range from GSM, 3G and 4G cellular communications, to Wi-Fi access and mm-wave wireless LANs, providing point-to-point and multi-point connections for voice and data, video distribution and Internet access. Convergence means that many products are already becoming multi-band multi-mode, not only using RF communications for voice and data transmission using many different standards and frequencies, but also for localisation and navigation purposes (e.g. GPS). As a result, many of them feature multiple air interfaces and advanced antennae systems.

The higher bandwidth demanded by services such as video-on-mobile and TV-on-mobile requires higher frequency wireless links, while the need for handheld mobile devices to operate from smaller battery packs demands low-power wireless operation. Simultaneously achieving these objectives requires innovation in the analogue RF front-end section (active and passive functions) as well as in the digital sections to achieve higher processing speed and computing power for lower power consumption.

Most of these RF devices need the support of a wireless infrastructure such as a base-station network for mobile phones or the transmitter network for digital terrestrial TV. With the world-wide expansion of mobile phone networks and wireless Internet access, there is very rapid growth in the base-station market. Because these base-stations have to simultaneously support a large number of transmission channels, they require high-bandwidth tuneable RF power amplifiers with very high linearity and high operating efficiencies. The main challenge here is achieving reliable, robust and cost effective technologies (long lifetime) for use in front-end circuits for mobile communication base-stations and wireless point-to-point and multi-point broadcast systems.

Many of these local infrastructures link into global infrastructures that carry data over vast distances via satellite, micro- and mm-wavelength links or optical fibre networks. These global networks require extremely high performance (high frequency) technologies, the main challenges being the development of high-speed circuits and technologies operating at frequencies up to 80 GHz and beyond.

There is also a local networking (access) requirement for broadband access in offices and homes via standard copper (telephone) wires. In practice this means a mixture of wired and wireless interfaces operating at various levels. The main challenge here is the reuse of standard technologies in volume production enabled by integration of new devices (such as LDMOS transistors) to enhance driving capabilities at low power. There are systems appearing for data transmission via standard copper power lines (AC line power cables), where the main challenge will be extending bandwidth and frequency.

In addition to communications systems, high frequency (micro- and mm-wave) devices and systems will become increasingly important in other applications. Emerging examples include short-range collision avoidance and road-safety systems in vehicles (at 24GHz, 77GHz and 110 GHz), radars and imaging devices for aircraft take-off and landing safety systems and imaging systems for access control and the detection of metallic and non-

metallic materials (explosives, ceramic weapons). This will involve the development of high-speed spatial resolution short- and medium-range sensors, radars and imaging systems operating at frequencies up to 1 THz. In the area of sensing, mm-wave spectroscopy is still in its infancy but initial applications in chemical analysis are emerging. The main challenges are achieving the required frequency and bandwidth and reducing sensitivity to effects such as humidity, temperature and mechanical impact.

Priorities for circuits and systems

- Increase the high-frequency capabilities of semiconductor processes to enable more computing power and/or the running of systems at higher frequencies for better precision
- Increase power efficiency and reduce power consumption (e.g. leakage currents) to achieve longer standby and operating times
- Decrease noise and other spurious effects to allow higher RF integration in standard CMOS
- Improve process/device tunability to meet the needs of a broader spectrum of applications
- Reduce form-factor in RF architectures
- Develop high-performance, small size, low cost circuit functions based on new passives, especially those that exploit low power and/or high frequency electro-mechanical signal processing capabilities of RF MEMS technologies, and other devices that have a direct impact on the development of new circuit architectures.
- Develop technologies for integration (including 3D integration) of RF building blocks (passive and active) into SiP modules
- Develop re-configurable RF circuits and 'dirty RF' with digital compensation/calibration for 'Digital Radio'.

Priorities for devices

- Develop models for components and devices at frequencies up to mm-wave frequencies.
- Improve CMOS and BiCMOS technologies to achieve higher integration levels
- Develop high-efficiency RF MEMS and filters, high-Q inductors, tight tolerance capacitors, high-density capacitors and low loss switches to enable novel and improved RF transceiver front-ends
- Optimise GaN and other III/V technologies for more efficient RF power applications
- Develop technologies for the integration of heterogeneous RF components onto silicon or into packages
- Improve technologies for multiplexing and interconnectivity with optical-electronics
- Extend III/V and SiGe technologies up to 1 THz
- Optimise antennae architectures on-chip and/or on-package (e.g. multi-beam)

Priorities for interconnection, packaging and antennae

- Carry out implementation studies into compact antenna systems and power amplifiers
- Develop on-chip and chip-to-chip RF connections (e.g. transmission lines) with reduced losses for high-speed applications
- Develop and exploit 3D integration technologies (chip stacking, wafer stacking and full monolithic integration) both for MtM applications with high performance and, especially, increased functionality per volume (e.g. 3D integration of functional layers realised by various technologies)

High-voltage and power

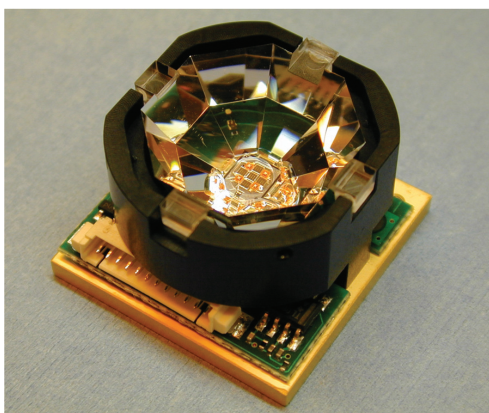
High-voltage (HV) can be defined as any voltage higher than that used for classical digital input/outputs (I/Os) in state-of-the-art semiconductor processes, i.e. starting at 3.3V or 5V. HV interfaces and functions are important parts of most (small) systems, usually as part of an I/O system that interfaces the system to the real world. They are typically needed when the I/O device requires a high power or high voltage drive (e.g. electro-mechanical actuators or LCD displays), or when high-voltage capability is required to protect sensitive circuitry from voltage spikes in electrically harsh environments - e.g. in automotive equipment. High voltage capabilities are also required in power management, power conversion and power distribution circuits. Power handling and power management is needed to drive low voltage CMOS circuitry from battery or AC-line power sources in a wide range of consumer products. Automotive systems need to drive electro-mechanical actuators such as fuel injec-

tion systems, solenoids, starter motors and electric windows.

High-voltage and high-power technologies can also help to solve some important social, environmental and economic problems, in energy generation, healthcare provision and emissions reduction. A few examples are discussed below.

Solid-state lighting (SSL)

Based on semiconductor, organic or polymer light-emitting diodes (LEDs), SSL will eventually replace both incandescent and fluorescent light bulbs because of its very high energy-efficiency - it produces around 40 lumens per watt compared to 14 -20 lumens per watt for incandescent lighting. In addition, SSL has a lifetime of 50,000 hours or more and it has excellent resistance to shock and vibration, all of which significantly reduces maintenance costs. SSL is already used in high-reliability applications such as traffic lights and is beginning to penetrate the home/decorative lighting market. It is also highly controllable in both intensity and colour, enabling the production of smart lighting systems that will depend heavily on HV and power technologies.



High-intensity solid-state lamp

Medical Ultrasound

The ability to drive 100 - 200 volts at a frequency of several megahertz will improve the speed and performance of ultrasound scanners. The ability to process high-voltage signals using high-performance analogue integrated circuits with high linearity and high frequency stability is a key requirement for improving ultrasound image quality.

Automotive

In the automotive industry, the driving forces are pollution and fuel consumption reduction. In addition to electric and hybrid vehicles, a lot of research activity is taking place to improve the efficiency of existing power trains. In combustion engines, both diesel and petrol, this has already resulted in the development of electronically controlled direct fuel injection systems based on solenoid actuators, increasing the injector drive voltage to between 80 and 150 volts. To implement ultra-fast multi-point injection systems, it may be necessary to move to piezo-electric injectors, for which drive voltages will increase to around 300 volts. For hybrid cars, high-power electronic systems will be needed to optimise overall efficiency, adjusting the relative torque produced by the electric motor and combustion engine, and recovering energy during braking. The standard hybrid drive train system already includes a high voltage battery pack (150 - 300 volts), the main inverter for traction (400 - 600 volts), and the buck and boost DC/DC converters for auxiliary loads (for example lamps) and for the inverter supply. For new power train systems an updated HV-Power silicon technology will be necessary allowing higher integration to minimize the cost and the wiring, and to increase reliability and electromagnetic compatibility.

Energy scavenging

Many of the autonomous devices that will lie at the heart of future ambient intelligence environments will need to scavenge energy from their surroundings in order to eliminate or reduce the need for battery replacement. This means tapping into energy flows such as those associated with movement, temperature differentials, pressure changes using electrostatic, magnetic, piezoelectric or magnetostrictive devices. Battery elimination is also seen a good way of reducing toxic waste.

Priorities

- Reduce transistor on-state resistance (R_{on}) to reduce power losses and improve breakdown

voltages
- Optimise R_{on} versus voltage
- Improve switching performance for higher switching efficiency
- Improve electrical robustness (e.g. reverse voltage, ESD) and operating temperature range
- Improve integration density of HV components
- Reduce parasitic effects
- Develop high-voltage/high-current interconnect architectures with thick Cu metallization
- Develop multi-level thin/thick Cu metallization
- Develop new isolation technologies, such as selective SOI, to allow more flexible integration of HV devices with CMOS, lower leakage, and higher operating frequency
- Develop energy scavenging systems for autonomous systems

Electronic imaging

Electronic imaging is now part of everyday life. Imaging technology, developed in synergy with memory and computing technologies, has opened up a wide range of applications. Market analysis shows that the number of applications will increase, with consumer applications will requiring a larger number of dedicated imagers per system. The image sensor business is strong in Europe and should continue to develop favourably.

Key applications include visible-light imaging for multimedia and industrial applications, X-ray imaging for healthcare (e.g. cancer diagnostics) and infrared imaging for rescue and emergency service cameras. Many of these applications require image sensors tuned to detect specific spectral wavelengths. Extending wavelength detection in the electromagnetic spectrum to sub-millimetre wavelengths (detection of terahertz radiation, which is a section of the spectrum between microwaves and far infrared light) will also open up new market opportunities. Finally the imagers of the future should have low power consumption, and be compact and easy to manufacture.

For visible-light imaging, the market driver is the camera phone, which currently represents 80% of the visible-light imager market. In 2006, approximately 1Billion camera phones were sold with a market growth rate of 30%. R&D is still needed in order to ensure competitiveness in both overall electro-optical performance and costs of the micro-cameras used.

Even though volumes for professional imaging applications such as space, military, medical and scientific imaging are lower, they nevertheless represent a large turn over. Currently, pixel sizes for these applications can be as small as 1.4 x 1.4 micron. Lowering the pixel size is mainly driven by cost at the device and system levels. However, it is becoming a real challenge to detect photons while decreasing pixel size. The nano/micro-electronics industry therefore needs to carry out R&D on new pixels architectures in order to achieve further pixel size reduction. The same trend applies to non-visible imaging. Polyamide filters, optics and overall assembly cost also represent a large part of the cost and are therefore still a limitation. Finally, co-design of the imaging pixels and the whole imaging system (including software) is becoming more and more important to efficiently address present and future market needs.

For non-visible imaging, different technologies are needed for different wavelength ranges. In addition to performance improvements that are common to all imagers, such as better sensitivity, dynamic range and endurance and lower noise and pixel-to-pixel crosstalk, there is a definite need for multi-spectral analysis using a single sensor technology.

In particular, terahertz radiation is a part of the spectrum that has not been adequately covered yet, even though there are many potential markets for terahertz radiation imagers. Targeted applications include surveillance systems to detect concealed weapons in airports and public places, industrial food inspection, and medical diagnostics. Some systems do exist, but these are based on cryogenically cooled devices and single diode detectors that need to be scanned in order to form a 2D image. Further research is therefore required.

Priorities

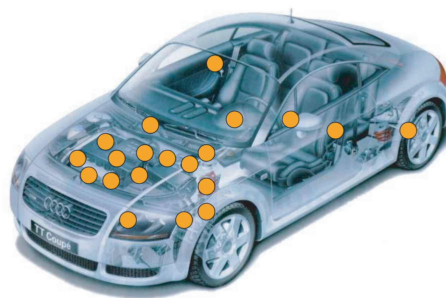
- Increase quantum efficiency of pixels and decrease

crosstalk between pixels with new micro-/nano-electronic processes
- Decrease noise sources in the driving electronics
- Develop pixel concepts for high sensitivity and very high dynamic range (more than 120 dB)
- Improve colour filter concepts to make them better suited to micro-/nano-electronic processes
- Develop plasmonic concepts to improve filtering and photon collection (see 'Beyond CMOS')
- Develop biomimetic /neuromorphic concepts for very high speed and very low power consumption
- Develop on-chip micro-optics (including micro-mirrors)
- Develop microsystem techniques to make micro-cameras (wafer level packaging)
- Create multi-spectral imagers from UV down to terahertz
- Develop 2D sensitive real-time room temperature monolithic imagers for terahertz imaging and spectroscopy

Sensors and actuators on CMOS platforms

Sensors and actuators are used almost everywhere to sense and monitor parameters and to correspondingly control actions of importance and interest in our daily environment. They play an essential role in interfacing electronic systems to real-word users and environments. Due to the large volume and variety of devices required to perform the different functionality requirements, the sensor and actuator market is huge. However, most of today's devices are stand-alone and are controlled and supported by vendor-specific electronics.

Since all sensors and actuators require control electronics to support their functionality, there is significant interest in integrating CMOS into sensor and actuator packages to improve performance and yield, and reduce cost. Monolithic integration also offers the possibility of putting a large number of sensors or actuators in a very small area. Although it would often be advantageous to monolithically integrate the sensors and actuators onto a CMOS support chip, in many cases the fabrication processes and materials used to produce the sensor or actuator are not compatible with CMOS platforms. Even when such integration is possible, device and system performance, device compactness, yield and cost need to be considered when deciding between a hybrid versus a monolithic approach.



Sensors and actuators are everywhere

The integration aspects (monolithic/hybrid) of sensors and actuators onto CMOS platforms will be an important challenge and focus for the years to come. This will include the development of sensors and actuators based on materials other than silicon (for example, III/V or plastic materials) that offer new functionality or lower cost, as well as arrays of sensors and actuators of the same or different functionality. In addition, new sensor types such as nanowires and carbon nanotubes with potential for improved sensitivity need to be investigated and fabrication processes have to be developed to integrated such new sensing elements into devices, systems and applications.

For this approach the CMOS platform as well as the sensors and actuator device wafers would be processed independently and hence their fabrication processes, materials and performance could be optimised independently. This also avoids the need for process compatibility. The greater challenge is full wafer or chip to wafer transfer and bonding of the sensors and actuators onto the CMOS platform. Developing high yield wafer-to-wafer transfer and bonding techniques will allow large-scale low-cost manufacturing. The chips can either be placed side-by-side or stacked on top of each other. Single chip to CMOS platform transfer and bonding will be an alternative approach for low volume or multi-functional

sensor and actuator devices transferred onto a single CMOS platform.

More research effort is needed for nanoscale sensors (see the section on 'Beyond CMOS'). Silicon nanowires and carbon nanotubes (CNT) show considerable potential for use as strain and deflection sensors, with high gauge factors being reported for experimental structures. The major challenge is large-scale, well-controlled fabrication and integration of these nanoscale structures into sensor devices.

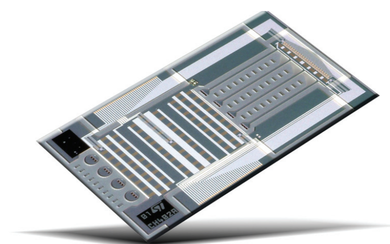
Of high importance for MtM is interfacing the extremely small signals generated by these nano-scale devices to micro-scale electronics. New analog circuit interfaces will be needed to exploit the extremely small signals from nano-scale sensors and NEMS operating as individual devices or dense arrays.

Priorities

- Monitor and assess different sensing principles and technologies with respect to applications or systems
- Reduce cross-sensitivity to non-primary meas urement parameters; e.g. temperature, light
- Identify the noise sources in the system and increase signal-to-noise levels
- Increase primary measurement performance in terms of accuracy, resolution, dynamic range, linearity, repeatability, operating range, bandwidth, response time, long-term stability, reliability and safety
- Co-design the sensor with the electronic circuitry, including the necessary read-out electronics (excitation, modulation and/or electronic feedback systems)
- Improve manufacturing methods for sensor calibration, e.g. trimming
- Increase robustness to harsh environments, e.g. dust and dirt, temperature extremes, humidity
- Reduce power consumption and increase power efficiency
- Reduce physical system size

Biochips and microfluidics

Over the last decade, micro/nanotechnology has become a powerful enabler of innovation in biological and biomedical applications. The marriage of micro/nanoelectronics know-how with biology, biochemistry, chemistry, and medical sciences will create major opportunities to revolutionise biology and medicine. Micro/nanotechnologies offer powerful ways to bring added value, in terms of cost, reproducibility, sensitivity, automation, analysis and new functionality in healthcare applications such as in-vitro diagnostics, drug delivery and minimally invasive disease intervention, as well as in environment control (water, air, soil), agriculture and food, defence or homeland security. A wide range of sensor types will be required, such as biochemical sensors, sensors for liquid and gas spectroscopy, ion-sensitive devices and sensors for detecting parameters such as CO_2 levels, ozone concentrations, fuel and oil conditions, hydrocarbons and gas.



Silicon-based 'Lab-on-a-chip'

Biosensing and bioanalysis are experiencing a paradigm shift in which complete biological assays are integrated into a single device, such as a disposable cartridge with an embedded 'lab on a chip'. Such cartridges will typically be hybrid components, in Integrating many different devices and materials, such as silicon chips, plastics and glass. For these applications, silicon chips will not only provide the brains for the system, but also offer attractive manufacturing processes and biocompatibility. Adding more functions on silicon to create highly heterogeneous integration means to developing techniques for chemical surface engineering, biocompatible packaging, microfluidics, electrochemistry, nanostructures and integrated optics. In particular, fluid handling at chip level will present a major challenge.

Priorities

- Develop microfluidics technologies (e.g. microvalves,

micropumps, fluid handling, fluidic connection, electrowetting)
- Develop biocompatible and low temperature packaging processes
- Control specific chemical functionalisation on full wafers before dicing
- Develop embedded reagents processes on chip
- Develop fully integrated biochips and biosystem in package solutions including signal processing, energy control, data treatment and data transmission
- Develop biocompatible materials and processes
- Develop free labelling detection with nano technologies (e.g. nanowires, CNT)
- Increase biosensor sensitivity and specificity

System-level co-design

Among other things, the success of MtM technologies depends on the availability of system-level co-design methods and tools. Even for digital IC technology, which has a long history of electronic design automation (EDA), we are far from using the capabilities of the latest CMOS processes effectively. The productivity gap between what you can put onto silicon and what you can design onto silicon is still growing. The reality is even worse for MtM technologies, because there is not only a digital design gap but also a multi-domain aspect to consider. State-of-the-art MtM design tools must therefore be a mix of tools that cover all technologies used in a single product, and are therefore likely to come from different vendors and have different levels of maturity.

For many of these tools, the ability to conduct accurate (qualitative and quantitative) and efficient simulation has yet to be developed. In addition, these tools are often closed proprietary systems with specific workflows, varying from vendor to vendor. Considerable effort must therefore be spent on adapting workflows and interfaces to fit the tools. The heterogeneity and span of technologies covered by MtM, together with the almost infinite ways in which they are combined to create new products calls for a paradigm shift, moving from design space exploration to system space exploration. Only a system-level approach will give designers the freedom to chose between different predefined and qualified technologies in order to produce products that are optimised for performance, cost, reliability and time-to-market.

The ultimate objective is to develop an open, unified, design environment. This would lower the costs and associated risks for industry, especially strengthening SMEs. An open environment is also an ideal platform for academia, simplifying the exchange of knowledge and results and providing unlimited customisation possibilities - something that is of particular importance at the forefront of technology.

Also essential is the development of an integrated co-design framework to allow the creation, simulation and optimisation of designs that not only span a broad range of MtM applications, but that also incorporate different processes (from wafer processing to assembly), different technologies (semiconductors and other application knowledge) and different disciplines (e.g. electric, mechanical, thermal, optical, bio).

The purpose of DfM is to accelerate process ramp-up and to enhance process yield, robustness and reliability. Priorities include enabling random and systematic yield loss estimation from design through yield models, and the creation of process-aware design flows, enabling yield optimisation early in the design flow and a reduction in costly design iterations.

Design for Reliability (DfR) is aimed at the accurate prediction, optimisation and up-front design of reliable products and processes; it is also often referred to as virtual prototyping. DfR requires a range of research activities, including the gaining of a basic understanding of materials behaviour and degradation/failure mechanisms under multi-loading conditions through accelerated reliability qualification tests and advanced failure analysis. This needs to be done with the benefit of various accurate and efficient multi-physical and multi-scale simulation models that can help to predict failure evolution. Detailed priorities are given in the section Heterogeneous Integration.

Design for Testability (DfT) aims to secure functionality,

quality and reliability before product release rather than after it. It is a challenging issue especially for MtM applications where multi-function products are built using multiple technologies, and where test strategies, methodologies and equipment need to be further developed.

Cross-cutting issues

Due to the trends in MM and MtM there is an increasing requirement for equipment development to be closely aligned to technology, with special equipment needing to be developed in order to ensure product manufacturability on an industrial scale. This requires close collaboration between product/process developers and equipment manufacturers so that the right balance between specialisation and sufficiently large-scale production can be achieved.

For MtM, material science plays an essential role. To some extend, the success of MtM will depend on a profound understanding for the properties and behaviour of materials and their interfaces under manufacturing, qualification testing and use conditions, and on the ability to tailor the material design for the requirements of specific applications. This issue is already acute for MM technologies, where multi-scale size effects and multi-material compatibility, stability and reliability will be key to success. Among the many challenges, characterisation and modelling of materials and their interface behaviour need more attention, especially for multi-scale, multi-physics and time dependent situations.

Novel MtM technologies will have strong interaction with 'Beyond CMOS' technologies. At the moment, one can actually buy a handful of electronic products made with carbon nanotubes (CNT). Examples are CNT sensors, probe tips and transparent conductive films. As one of the novel solid materials, nanowires have also received much attention from the R&D community as components for electrical circuits, sensors or light-emitting sources based on CMOS compatible processes. Although the R&D activities for CNT and nanowires were initiated to address the future need of IC technologies beyond the physical limits of CMOS, more and more R&D activity nowadays is devoted to using CNT and nanowires to create MtM products. In return, this increasing awareness and interest in developing and using 'Beyond CMOS' technologies to broaden MtM applications will also speed up the success of beyond CMOS for More Moore.

Implementation

MtM is much more than just miniaturisation. It is simultaneously coping with the multiple complexities of functionalities, design requirements, disciplines, scales, technologies, materials, material interfaces, processes, damage / failure modes and variability. MtM is also much more than just technology. It is multi-application, multi-market, multi-infrastructure, multi-billion dollar investment, multi-supply chain and multi-business model. The continuation of Moore's Law has been enabled by an excellent ecosystem consisting of public awareness, the availability of resources (e.g. qualified human capital, materials, finance), the existence of R&D infrastructures, manufacturing facilities and supply chain networks, and market maturity. Therefore, the success of MtM depends on not only the availability of the needed technologies and competencies, but also on greater social awareness, new industrial visions, strategies and business models in which the total value chain has to be optimised according to the characteristics and needs of the target application. The following issues need special attention.

Partnerships between electronics players and non-electronic players are essential at all levels (industry, research institutes and public R&D organisations). In the past, much of the electronics industry has abandoned a vertical business model and focussed on its own core business. However, while business competition between them has intensified, collaboration in pre-competitive technology development has become common practice. For the MtM business, there is a clear need to standardise and commoditise the associated technologies and design methodologies to enable fast ramp up to economic scale and fast product implementation. This can only be achieved by establishing and intensifying structured collaboration within the electronics sector and, equally importantly, between the electronics sector and non-electronic sectors (such as healthcare). For

MtM related technology and new product development, it is essential to understand the marketing needs/trends, master the associated application knowledge, share the R&D costs, and be able to access the associated markets that are beyond the existing operating fields of electronics industries. By joining forces with application sectors, it will not only be possible to enlarge existing markets (such as automotive). It will also be possible to drive and speed up the emergence and growth of new high-tech markets (such as in safety, personal wellness, and solid-state lighting).

There is a clear need to strengthen structured cooperation between industry and the academic community. The associated benefits are twofold. Firstly, it will help to speed up the creation of fundamental knowledge in order to meet the urgent needs of MtM technology and business. Close collaboration between industry and academia will increase investment in knowledge development and improve the efficiency and industrial relevance of fundamental research. Secondly, it will greatly increase the success rate of innovation. Over the past two decades, the academic community has spent a lot of effort working on specific MtM related technologies and products (for example, sensors and MEMS). However, technological feasibility and IP do not always guarantee business success. Often, the industrialisation and commercialisation of excellent R&D results requires joint competencies and effort from both industry and academia.

Cooperation between multi-national corporations and SMEs is also important. Due to application diversity and a plethora of unsolved challenges in MtM technology, it is a perfect playground for highly innovative SMEs to play an essential role in developing MtM-related IP by exploring both evolutionary and disruptive technologies. SMEs can also contribute to market scouting and market development by quickly bringing small numbers of prototypes and products to users and serving low-volume application needs. However, SMEs alone cannot push MtM technologies and products into mass consumer markets without the leading electronic industries committing their resource and capabilities. Collaboration between multi-national corporations and SMEs will speed up the development of new technology and new markets and broaden application scopes.

It is also essential to develop and implement suitable business models for MtM business creation. Due to the inherent multi-dimensional complexity of MtM technologies and its strong application dependency, the existing business models for 'Moore's Law' type industry are not automatically transferable to the MtM industry. Several elements have to be considered in defining MtM business models. Firstly, with more functions being integrated into one (sub)system, the business scope of all parties involved in the product value chain may change, and their profitability partition may also shift. This may lead to changes in the industrial landscape and competitive balance. Secondly, new and quantitatively reliable cost models will have to be developed. Currently some of the underdeveloping MtM technologies have unclarified cost consequences. At the same time, for many MtM technologies that are about to be adopted, the cost of integration is not always known - for example, the Known-Good-Die (KGD) solution.

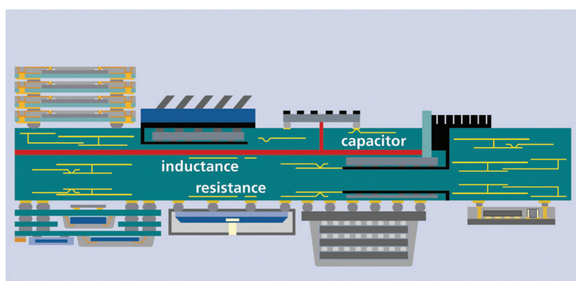
Supply chain management is another non-negligible element, because of expanding but not yet mature MtM markets and the non-consolidated roles of a large number of industrial players. For high-volume MtM products, cost competitiveness and short time-to-market are the determining success factors. Winning business models needs to integrate and optimise all these important, interlinked and sometimes controversial requirements.

Due to the tremendously broad application scope of MtM technologies, it is not cost effective to develop individual technologies for each application. The business success of MtM depends on the ability to combine application-specific needs with cost and time-to-market requirements. Therefore, it is vital to develop system architectures, co-design methods and tools, generic design platforms and design flows, effective standards, re-use technologies and modular processes.

Domain 'Heterogeneous Integration'

Rationale

The future of Nanoelectronics will see a combination of 'More Moore' (MM) and 'More than Moore' (MtM) components, integrated together in the form of 'System-in-Package' (SiP) solutions. SiP is defined as multi-functional systems built up using semiconductor devices and devices based on other technologies into packages with IC (Integrated Circuit) dimensions. SiP focuses on achieving the highest value for a single packaged microsystem. The concept applies to diverse technologies and application areas, ranging from sensors and actuators to RF modules for mobile communication, solid-state lighting, and even healthcare devices such as biosensors. To distinguish between various SiPs, they can be classified into three categories. The first category refers to packages that contain multiple dies - for example, Multi-Chip-Modules, Package-in-Package and Package-on-Package. The second one refers to sub-systems built up using more than only IC processes, such as passive integration. The last one refers to micro/nanosystems with more than one electronic function, built using multiple technologies. With such a SiP, the application benefits from a comparable level of miniaturisation to that achievable with a SoC solution, together with the enhanced functionality enabled by MtM solutions. SiPs also benefit from having each part of the system fabricated in an optimum process technology.



The complexity of heterogeneous Integration

Generally speaking, SoC and SiP technologies are complementary (not competing) approaches to realising customer value. They are synergistic in nature, which means that SoCs can be components of SiPs. The decision on which approach to use (or how to partition the system between them when both approaches are possible) is based on a thorough assessment of development and manufacturing costs and a realistic market assessment. Rather than arguing about which is better, it is better to leverage both capabilities in order to achieve maximum advantage.

The key technology underlying SiP is Heterogeneous Integration (HI). HI not only allows the integration of multi-functional components into one package. It also provides an interface to the application environment. It therefore includes the 'glue' between the world of nanoelectronic devices and systems that humans can interact with. HI has to ensure the practicality of integrating components based on different technologies and materials. For example, an ultra-miniature single-package bio-sensor might contain photonic components for detection, RF components (using InP or GaAs) for communication, logic components for data compression and energy scavenging or energy storage components (thermo-electrics, fuel cells, thin-film batteries) for power supply. And because the reliability of such systems will be increasingly important, future HI technologies will have to achieve failure rates measured in parts per billion rather than today's parts per million. Another driver for HI is the shorter time-to-market and the manufacturing flexibility compared to SoC solutions. The high degree of flexibility in HI makes it possible to integrate multiple proven SoC and MtM solutions in a single subsystem.

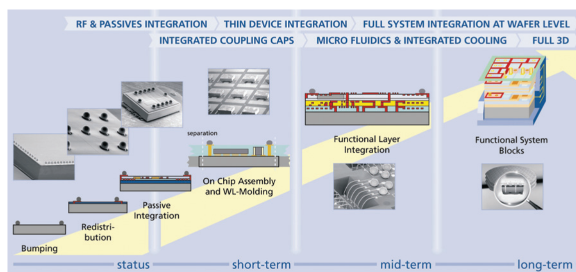
Research priorities

The present status of system integration is still largely dominated by single-chip packaging, although the percentage of multi-chip/multi-component products is increasing rapidly. Most of the latter are stacked-die SiPs based on conventional wire bonding - an approach that will not be sufficient to meet the multi-functional integration requirements of advanced SiP solutions.

Wafer-level integration

Future systems will require non-electronic functions enabled via the use of alternative materials and

processes. However, integration of these alternative materials and processes into conventional semiconductor processes often reduces yield and/or increases cost, as well as introducing many technological challenges. Ultra high-density wafer-level integration technologies must therefore be able to successfully combine different technologies while also meeting yield and cost requirements.



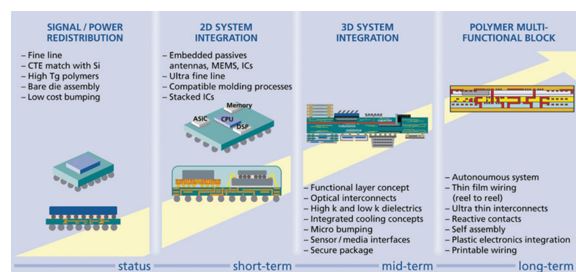
Roadmap for Wafer-Level Integration

Firstly, wafer-level integration has to maintain compatibility between the first-level interconnect with the 'back end of line' (manufacturing operations performed on the semiconductor wafer following first metallization). For embedded devices, wafer-level integration may these involve using layer deposition techniques to create embedded components, embedding ultra-thin devices into cavities or polymer layers, creating high surface-area honeycomb structures for integrated capacitors and fabricating nanowires to integrate III/V material (InP, GaAs) and SiGe components. Secondly, new technologies will be needed for wafer-scale integration of antennas (24 GHz to 80 GHz), photonic components, batteries and energy scavenging devices, bio-interfaces, micro-fluidics and MEMS. In addition, wafer-level encapsulation technologies using nano-filled materials (wafer moulding), alternative technologies for 3D-integration (for example, through-silicon via technology) and new isolation and shielding technologies for RF will have to be investigated. To reliably manufacture wafers with such a high degree of integration, advanced assembly, dicing and handling technologies for thin wafers and chips will need to be developed. Improved approaches for thermal management will also be required.

Module Integration

Future board and substrate technologies have to ensure cost-efficient integration of highly complex systems, with a high degree of miniaturisation and sufficient flexibility to adapt to different applications. Technologies for embedded devices such as MEMS, passive or active components, antennas and power management will be the key for highly integrated modules.

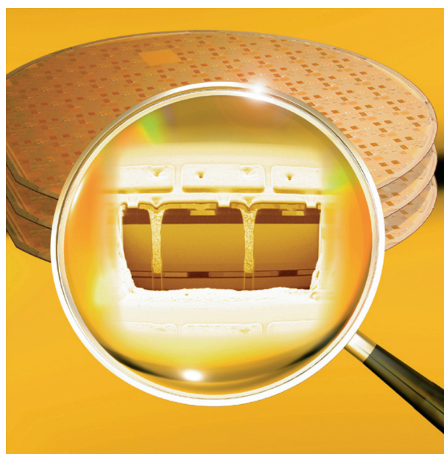
To reach this goal, new substrate materials, embedding technologies and encapsulation technologies have to be developed, such as high-K and low-K dielectrics, and tailored polymers (such as Tg, CTE, CME) that correct the mismatch between dies and substrates. In addition, finer lines and smaller vias for substrates and interposers should be made available at lower cost. Flexible substrates suitable for reel-to-reel manufacturing, integrated optical interconnects and photonic packaging will then be the next steps for future SiPs. In the long term, printable wiring and printable circuitry on organic substrates will increase productivity and lower environmental impact.



Roadmap for Module Integration

3D Integration

A promising solution to achieving a high degree of system miniaturisation and flexibility is 3D system integration - a technology that enables different optimised technologies to be combined together and that has the potential for low-cost fabrication through high yield, smaller footprints and multi-functionality. In addition, 3D integration is an emerging solution to the 'wiring crisis' caused by signal propagation delay at board and chip level, because it minimises interconnection lengths and eliminates speed-limiting intra-chip and inter-chip interconnects.



3D integration using through-silicon vias

Currently, vertical system integration uses through-silicon vias with a diameter of 2 microns. Using flip-chip technologies for multi-die stacking needs new approaches for vertical vias. Existing embedding technologies integrate active and passive devices into rigid or flexible substrates. One example of this is a process in which thin chips are die-bonded and embedded by laminating them in resin-coated copper layers, in which electrical contacts are created by laser drilling and Cu metallization. In another example, flip-chips with very thin interconnects are soldered or glued to flexible substrates, followed by embedding in an adhesive layer. In both cases, the chips end up fully integrated into a flat substrate, either rigid or flexible, onto which further layers can be applied or other components can be conventionally assembled. By using a thin flexible substrate, a 3D structure can be created by folding the substrate; this also leads to a decreased footprint. Package stacking offers high flexibility but a relatively low integration density.

Other research subjects are low-temperature wafer bonding, ultra thin wafer technologies that also address the issues of dicing and handling, thin interconnects, secure package technologies, integrated shielding (separating RF and Power), vertical chip integration, through-silicon vias / power vias, optical chip-to-chip interconnects, and integration of energy storage/conversion devices.

Interconnect, packaging and assembly

Interconnection, packaging and assembly are major bottlenecks for future nanoelectronics technology and business development. The result of ongoing trends in Moore's Law is the ultimate nano-scale CMOS silicon chip. However, nano-scale chips need nano-scale interconnects and nano-compatible packaging and assembly. Multi-functional SiPs need new system integration technologies, in which interconnect, packaging and assembly will also have to meet the needs of heterogeneity.

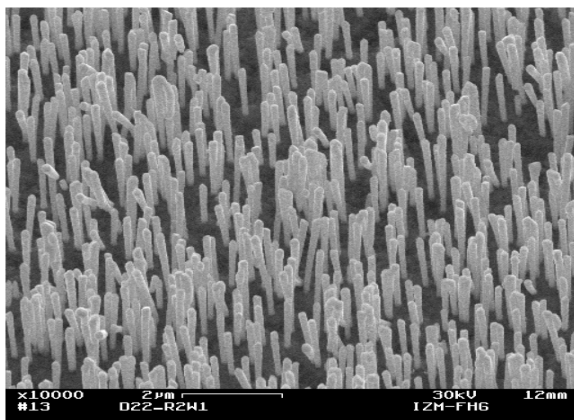
Due to the further miniaturisation and heterogeneous integration of SoC with SiP, the back-end costs (interconnect, packaging, assembly and testing) will increase significantly compared to current IC packaging technology. Due to the increasing power density in chips, there is an increasing requirement for low-cost reliable micro-bumps that can handle high current densities. Chip interconnects will also have to be developed that can withstand temperatures that may be in excess of 200°C. Next to that, there will also be a demand for low-temperature, solderless interconnect technologies and very low cost printable interconnects.

Future assembly and packaging technologies will have to support 3D technologies as well as being suited to low-cost, high-speed, high-precision assembly methods. Although appearing to have promising potential, new technologies such as printable interconnects, self-alignment and self-assembly will have to demonstrate their ability to allow high productivity at reasonable costs. Thin package profiles will need alternative encapsulation processes such as compression moulding, film coating or micro-encapsulation by jetting.

Nanotechnologies

In the mid-term (until 2013), nanotechnology will be used to optimise material properties, improve device functionality and create new interconnection techniques. In the area of improved materials, the addition of nanoparticles will provide a means of adjusting parameters such as electrical resistance, thermal conductivity, coefficient of thermal expansion, and coefficient of expansion due to moisture (e.g. for polymer materials). Nano materials will also provide new solutions for high-

k dielectric capacitors and low-k dielectric inductors, improving the quality factor of these components. Effective thermal management of multilayer systems will require the development of improved thermal interfaces. To understand materials with added nanoparticles or nanoscale pores, phononic effects will have to be studied. A better understanding of phononic effects will also enable improvements in thermal performance. In the area of interconnect and assembly technology, nanostructures will allow surface activated bonding and provide nano-pillar contact bumps.



'Nano-lawn' – nano structured metal surface for low temperature joining

In the long-term (from 2013 to 2020), nanotechnologies and nanostructures will be used to develop nano-interconnection and nano-assembly technologies. Possible applications include carbon nano-tubes (CNT) for heat dissipation and/or interconnects, low-temperature interconnects using nano-structured surfaces, self positioning/assembly of die/devices and molecular bonding.

Modelling, Simulation and Design

In future electronic systems, the technology boundaries between semiconductor devices, packaging, and system technologies will become indistinct. It will no longer be possible for package designers to design chips and systems separately. Silicon chip, packaging and system aspects will need to be considered together in an integrated way. As a result, a broad range of complex design parameters will have to be analysed in order to optimise system partitioning, with trade-offs between chip, package and system design. To effectively address this issue, a detailed physical understanding of the behaviour of material, IC, package and assembly technologies and their interactions in multi-physics domains is needed.
The parameterised models for chip, package and system-level co-design, covering aspects of Electro-Magnetic Radiation (EMR), Electro-Magnetic Compatibility (EMC) and other multi-physics requirements should be developed to address the 45-nm CMOS generations and beyond. For on-chip interconnects this will require characterisation for frequency spectra in the range 30 GHz to 80 GHz or higher, and for off-chip interconnect/packaging characterisation up to 40 GHz. This will allow full design synthesis, taking into account RF, thermal and EMR/EMC aspects.

The design of SiPs requires cross-disciplinary design capabilities, new methods and tools such as design rules, a 3D SiP design platform and a multi-technology system design tool. In addition, design rules for integration of MtM and ultra-miniaturised MM components have to be developed, for applications such as e-passports. In general, system partitioning, technology and design convergence have to be redirected to a manageable number of platforms with a high degree of standardisation and re-use, so that an economically viable industry can be built. In the area of Design for Manufacturability, designed to accelerate process ramp-up and enhance process yield, robustness and reliability, random and systematic yield loss estimation from design must be enabled through yield models. Process-aware design flows must be developed, enabling yield optimisation early in the design flow and reduction of costly iterations.

In the area of Design for Reliability, designed to predict, optimise and design up front the reliability of products and processes, the range of required research activities is extensive. Modelling has to be multi-scale integrated (from atomic to macro), multi-physics (e.g. electrical, mechanical, thermal, physics, chemical), multi-damage (e.g. cracks, delamination, fatigues, electro-migration, voids, creep, degradations) and multi-process (wafer, micromachining, packaging, assembly, qualification and application profile), and it must incorporate prior loading conditions in order to understand and predict per-

formance and reliability. As part of this work, new algorithms and simulation tools will have to be developed. Advanced failure analysis techniques and correlation methods are needed to localise multi-physics based failure modes and the associated process for MtM products, plus an understanding of the failure mechanisms and their interaction.

Innovative experimental methods and techniques are to be developed to extract material/interface and total system behaviour, in order to provide inputs for modelling and simulation on one hand, and to verify the modelling results and design rules on the other, covering both nano- and macro-scales.

Efficient reliability qualification testing methods and better understanding of the physics of failure-based correlation models are required for accelerated reliability qualification tests, as well as efficient optimisation methods for design rule development of non-linear and multi-parameter process/product responses.

Testing and Quality Management

Due to the higher value of an integrated system compared to a single component, quality management is becoming even more important. To guarantee quality, test procedures and test requirements must be considered during the design phase and integrated into the production flow.

For wafer- or die-level system testing, test and burn-in procedures for wafer-level SiPs, expanded later on with low-cost probes/contactors for massively parallel testing and RF and high speed mixed-signal tests, will ensure the quality of Known Good Die (KGD). Procedures and interfaces for RF and mixed-signal tests are also a high priority for module testing. Fully integrated test data diagnosis flows for SiPs, together with automated test pattern generation and tests for devices such as integrated sensors and fluidics, will ensure the (economic) testability of highly integrated modules. Furthermore, multifunctional SiPs in which several different technologies are used within one package pose many challenges not only in relation to test strategies and technologies for specific applications, but also in relation to test time and test costs. More effort is therefore needed to develop Design for Testability methods to secure functionality, quality and reliability before release.

For software testing, configurable functions that can perform extensive self-testing will be required. The semantics of these self-tests must be clearly defined and the results of individual functional tests should not depend too much on the order in which the tests are invoked. Advanced component- and aspect-oriented development methods will aid this process.

Cross-cutting items

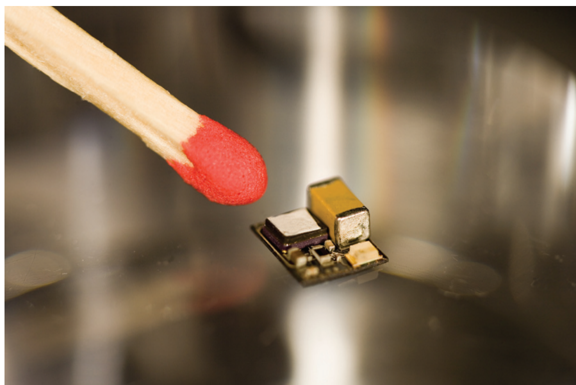
Heterogeneous Integration concepts must provide technologies at lower cost together with comprehensive risk assessment, shorter time-to-market and a higher degree of flexibility. A modular technology approach (such as a SiP toolbox containing materials, equipment, technologies, interfaces, test modules etc.) will be needed to achieve these objectives. Zero-defect technologies (both at package, chip and integrated system level) should help companies to create right-first-time designs. New integrated and low-cost cooling concepts will be needed. Secure package technologies will become a high priority. These technologies will have to provide evidence of tampering (or at least resistance) and related protection mechanisms to protect confidential information in secure applications will become a high priority. In addition, future HI concepts must take environmental issues into account. Chemicals and materials should have minimum impact on the environment and people. New concepts will also be needed for the repair and re-use of modules to assure long-term availability of SiPs (15 - 20 years).

Implementation

Clearly, the development of heterogeneous products with more than just electronic functionality needs to involve non-electronics companies in order to offer added value to customers. For such products, HI will be the bridge between electronics and applications. This trend towards HI will lead to a positive shift within the value chain of electronic systems from production of the MM components and MtM component right through

to integration of these components into a single package or total system solution.

Clearly, the development of heterogeneous products with more than just electronic functionality needs to involve non-electronics companies in order to offer added value to customers. For such products, HI will be the bridge between electronics and applications. This trend towards HI will lead to a positive shift within the value chain of electronic systems from production of the MM components and MtM component right through to integration of these components into a single package or total system solution.



Miniaturized module on silicon using via-in-via technolog

The future of electronics will be smart multi-functional systems linked into networks, containing both electrical and non-electrical functions and used in a variety of applications. HI is the key to integrating these functions into one system. For the fabrication of heterogeneous systems, new architectures and system integration technologies are necessary, which have to ensure the realisation of reliable systems with minimum size and at low production costs. Adequate interfaces for different application environments have to be created.

System integration and advanced packaging technologies are becoming the bottlenecks for the future of nanoelectronics. Due to the higher number of pins, reduced size and the integration of non-digital functionalities, the cost of testing as a proportion of total product cost will increase. Packaging and assembly also become more challenging due to the integration of new technologies. In addition, the realisation of these highly customised systems needs detailed knowledge about IC and packaging technologies and the application. Europe, with its strong position in both semiconductors and advanced application markets (for example, automotive, medical equipment and machinery) has ideal pre-conditions for a success in the HI field.

The focussed European research institutions (including several labs in leading industries) offers industry a full range of application-specific MtM solutions and leading HI technologies. Bringing together these strong R&D competencies and application knowledge will offer the greatest opportunity for success over the next decade. In that game, large electronic companies will provide solutions for high-volume products, while SMEs will successfully conquer niche markets.

An efficient infrastructure and joint commitment can support future compact system development in Europe. It is clear that no single company or EU country can solve all these technological and business challenges alone. However, a European network of product developers, device manufacturers and technology providers, united under the umbrella of ENIAC, will be able to provide the solutions.

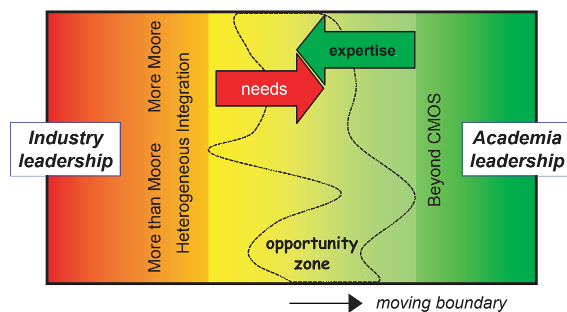
Domain 'Beyond CMOS'

Rationale

While the previous technology domains outlined short- and medium-term evolution in their respective fields, significant breakthroughs can be expected in the long-term from the progress in nanometre-sized functions. The interaction between classical approaches and 'Beyond CMOS' disruptive functions will offer significant opportunities for emerging markets. There is a continuous and moving boundary between classical approaches in the 'More Moore', 'More than Moore' (MtM) and 'Heterogeneous Integration' (HI) domains and the disruptive technologies 'Beyond CMOS' that nm-sized features will enable, complementing or replacing conventional silicon technology. There are thus significant opportunities for emerging markets where R&D organ-

isations, SMEs and start-ups, together with larger companies, will play a significant role.

The 'Beyond CMOS' domain in the present SRA is not limited to the research trends covered by the ITRS chapters on 'Emerging Research Devices and Materials' which mostly address devices and architectures for computation, storage, and information transfer. The present SRA also addresses the future of the MtM and HI domains. A special emphasis is put on the necessary co-development of emerging devices and of the associated system architectures needed for different applications. Cross-cutting issues such as manufacturing techniques, simulation, modelling and characterisation are then discussed. Finally, some conclusions on how R&D in this domain could be conducted at the European level are drawn.



Interaction between Beyond CMOS and classic approaches creates new business

Research priorities

Timeline for new concepts

Emerging devices are likely to be introduced initially in the form of low complexity blocks integrated into complex systems, before moving to more complex regular structures and, at a later stage, to complex random logic computing blocks. After the basic functionality of an emerging device (a 'Proof of Concept') has been demonstrated, it is expected that a few optimised components integrated into a system would be the next logical step. At this point, major issues will still need to be resolved regarding manufacturing techniques and the reproducibility of performance, as well as in terms of design methodologies and system architectures. MtM functionalities such as interfaces or analogue processing will be the likely entry point for these non-conventional components.

As the technology and its associated design techniques progress, more complex functions will be implemented, most probably in the first case as regular structures - e.g. memory arrays - where the learning curve is somewhat easier to climb. The introduction of emerging devices in complex computing systems - either as a complement to Si CMOS-based 'random logic' or as a disruptive new approach - is likely to be the last step in the introduction of the maturing technology.

A way for further computation scaling

The US Nanoelectronic Research Initiative (NRI) defined major research vectors for achieving further scaling of computing devices that are sustainable in the long term [13]. Some of the research directions will explore innovative ways to compute at low power consumption, either by using alternative schemes to encode information (using 'new state variables') or by operating out of equilibrium. Efficient information transfer via a mechanism other than the electromagnetic one is another major unsolved challenge. Finally, managing the heat transfer more efficiently through phonon engineering is looked at as a critical challenge and as a promising path for the future.

New state variables

Many different information carriers need to be explored in addition to charge and none of them currently stands out as a clear winner. Examples include spin, molecular state, photons, phonons, nanostructures, mechanical state, resistance, quantum state (including phase) and magnetic flux. In the following paragraphs some of these carriers will be detailed. However, the order in which they are presented does not indicate any specific priority or likeliness of success with respect to other candidate 'state variables'.

Spintronics (spin-based electronics) has many potential advantages, including low power operation, non-volatility and co-localisation of data processing and storage. Metal-based spintronics is likely to be first introduced for data storage applications using either spin torque

switching or domain wall effects. Semiconductor-based spintronics could find application in data processing, though major breakthroughs are needed in materials (e.g. semiconductors with a higher critical temperature), devices (e.g. injection/detection trade-off), co-integration with CMOS or in exploring promising physical phenomena (e.g. 'dissipationless' spin current). Spintronics using half-metals and molecules also need to be explored. It should be stressed, however, that no clear information processing device has so far emerged as a promising candidate to replace or supplement CMOS logic.

Molecular electronics is targeted at creating functional blocks at the molecular or supra-molecular level that could be assembled in more complex functions. Fully molecular-based complex systems including interconnected molecular logic and molecular memory devices have still to be demonstrated. Limited molecular logic, memory and interconnect functions have been shown, based on different types of molecules, but their integration into a single chip is still an issue. The first potential application is using the bistable behaviour of certain molecules to produce memories with an extremely high density. We are still at a very early stage, where the reproducibility of reported results is not always evident. Specific issues, such as contacting the molecule, carrying enough current to provide noise immunity and a reasonable fan-out, and the addressing and read out of specific blocks remain to be solved.

Information transfer

Although significant research is carried out worldwide on 'alternative' devices, no significant technological breakthrough has been achieved so far on information transfer in an integrated circuit. One of the more likely contenders to replace electromagnetic communication (i.e. information transfer through charge current in a metallic wire) is photon communication (i.e. light in the visible or IR range). More specifically, the very dynamic fields of nanophotonics, including plasmonics, allows the confinement and interaction of photons and electrons in a small volume, opening up the possibility of processing data at high frequency without compromising integration density. Roadmaps for this field of research are being proposed in the ETP PHOTONICS21 and in several European projects [14,15,16]. Further work is needed to assess the potential of such technologies in complex systems in terms of connection granularity, integration density, crosstalk, variability and power consumption.

It should be stressed that significant progress will come not only from breakthroughs in materials and device research, but more significantly from the creative interaction of technology progress with progress in layout, design, software and system research. For example, an optimised architecture through a better coding and localisation of data is likely to bring significant improvement in information transfer techniques. Finally, more disruptive approaches such as stochastic resonance need to be explored.

Heat transfer management

The emerging field of phononics aims to control phonon movement by using engineered nanostructures. It brings new opportunities in the interaction between quasi-particles (e.g. electrons, photons, spins) and phonons, potentially allowing better heat removal, isolation from thermal noise and better carrier mobility. Europe is well positioned with respect to worldwide competition in this field provided it continues to receive timely funding.

Enrichment of MtM and Heterogeneous Integration

While the roadmapping exercise for further computation scaling is fairly well on-track through ongoing work in the ITRS and NRI [12,13], a significant conceptual effort is still needed to define meaningful research vectors that look at how nanotechnologies could help to further enrich the 'More than Moore' and 'Heterogeneous Integration' domains. Special care should be taken to keep the field open to new 'out-of-the-box' ideas.

Because MtM and HI technologies are strongly application-driven, it makes sense to start from the societal needs, then derive generic macro-functions such as sensing and actuating, RF and/or optical external communication, energy management or bio-interfaces, and

finally analyse how nanotechnology-based solutions can significantly improve these macro-functions. Examples of application-driven devices can be foreseen in different fields. For example, using spin-torque for RF detection, plasmonics for more sensitive optical sensors, nanowires for single-photon secure optical communication, nanodevices for molecular recognition or nanostructured materials for enhanced energy efficiency. It is expected that such new ideas will move to the MtM and HI domains as they mature, in the same way that 'non-conventional CMOS' moved from the 'Emerging Research Devices' chapter to the 'PIDS' chapter of ITRS. Dedicated European workshops may help to refine this research structuring effort. At the same time, international acceptance of the methodology should be sought in forums like ITRS.

System architecture

At the device level, it is important to pay attention to the 'systemability' of emerging devices, i.e. the capacity of a device to be integrated into a complex system. An in-depth analysis of this concept has been carried out by the MEDEA+ Scientific Committee [17].

Moving up to functional block level, some emerging devices may offer new information processing paradigms by performing 'dissipationless' computation in limited domains where information carriers will not encounter scattering (in a 'ballistic' regime) or where phase information is maintained (as in quantum computing before de-coherence occurs).

Emerging devices are expected to be more defective, less reliable and less controlled in both their position and physical properties. It is therefore important to go beyond simply developing fault-tolerant systems that monitor the device at run-time and react to error detection. It will be necessary to consider error as a specific design constraint and to develop methodologies for error resiliency, accepting that error is inevitable and trading off error rate against performance (e.g. speed, power consumption) in an application-dependent manner.

Using a similar approach, analogue blocks of low complexity built with emerging devices may eventually find more extended use in balancing power consumption, in analogue-digital partitioning and in signal restoration.

Von Neumann architectures - or more generally, programmable digital systems - will have to be reconsidered, especially with respect to optimising the localisation of data processing and storage and in co-engineering the software and the architecture (e.g. parallel processing). However the legacy of more than 40 years of continuous development in classical electronic systems should not be underestimated.

Open issues such as giving up deterministic computation (e.g. in neural networks or DNA computing) or addressing emergent behaviour in complex systems are new exciting research fields where multi-disciplinarity is key.

Physicists, designers and system researchers cannot afford to work in isolation any more, focusing on their own field and having well-defined interfaces and handover mechanisms to other areas. The main challenge is to close the triangle between applications, emerging devices and design resource constraints in order to manage complex interaction between the different levels of system development. It is therefore essential to develop real multidisciplinary cooperation between all those stakeholders who play a part in optimising the overall performance of a system.

Manufacturing opportunities

As we approach the nm scale, the ability to manufacture billions of devices on a chip while maintaining full control over their properties is an overwhelming challenge that will probably lead to unbearable development and production costs. While it is difficult to predict which new processes will make their way into future manufacturing lines, there may be a comeback for chemistry [18], especially as development of the so-called 'supramolecular toolbox' progresses and selective processes (e.g. surface functionalisation) become more commonly used. Directed self-assembly (a 'bottom-up approach') and possibly bio-inspired and templated assembly are attractive concepts for low-cost manufacturing that need further investigation, although the fab-

rication of complex non-regular integrated systems has still to be demonstrated. Bio-inspired manufacturing processes may be useful to address defect-resiliency and the self-repair of defective systems.

It is probable that future successful technologies will combine novel bottom-up and more traditional top-down manufacturing to achieve increased performance and cost effectiveness. Finally, as discussed in the previous paragraphs, research into new architectures may also help to relax the need for a deterministic approach to controlling the properties of the elementary devices.

Cross-cutting issues

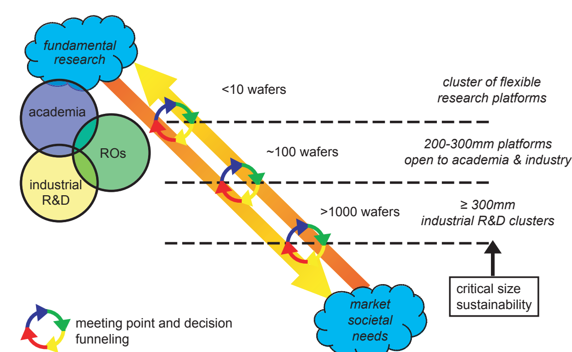
Statistical characterisation of complex systems that use emerging devices is a major challenge that is far from being solved, though continuous progress is being observed in that direction. It is necessary to evaluate nm-sized features on a mm-scale, analyse single objects in three dimensions, including defects, and pay special attention to surfaces and interfaces. It is important to extract a full set of critical parameters, such as structure, composition, charge density, chemical conformation, etc. It is even possible that we do not currently know what critical properties to analyse in emerging devices. In performing these analyses, it is also important to bear in mind the throughput and cost effectiveness needed to handle the huge database of information that must be managed and analysed.

Abstracting the behaviour of emerging devices through simulation and modelling will require major developments in which Europe can play a significant role. The development of early models is mandatory for co-engineering devices and systems. Techniques that are less common in nanoelectronics, such as the combinatorial approaches used in the pharmaceutical industry, will require an extensive set of experimental data that may be lacking, especially at a very early stage of the research. In particular, safety and environmental issues have to be addressed from the beginning if there is a likelihood that nm-sized particles could be released during the lifetime of the system or during recycling processes.

Implementation

Looking at the continuous stream of hype related to nanotechnology and emerging devices, the challenge is to select promising techniques early enough, while still keeping an open mind about disruptive ideas at all times. There is also the challenge of making the overall process time- and cost-efficient, while at the same time promoting cooperation, competition and diversity among the research teams in Europe.

The process of narrowing down the number of options will have to reach milestones, where the capacity to integrate emerging devices into complex systems is assessed. Narrowing down the options should be done at successive decision points before moving on to the integration of new devices into more complex systems and before committing to R&D costs order(s)-of-magnitude higher. These decision points will provide a reality check for new ideas by bringing together material and device scientists, function designers and manufacturing experts to assess them. Through this process, ideas will be progressively brought into industrial relevance. Better involvement and networking of the different stakeholders from academia, major research organisations and industry should be encouraged and organised, adopting a similar approach to the US NRI initiative by involving industry through the SRC and academia through the NSF as a possible way forward.



Narrowing the number of emerging options goes through assessment milestones

Different European research infrastructures successively address the growing challenge of demonstrating the

integration of innovative concepts into complex systems. Public and private stakeholders should make sure that at every stage of emerging device assessment and integration these infrastructures are not only well coordinated, but that they are also viable for state-of-the-art investment and have efficient running costs.

Multidisciplinary research in the 'Beyond CMOS' domain will also bring new challenges in education and training. It should allow researchers working in different fields to understand one another's language, working paradigms and way of thinking so that they can interact efficiently across radically different domains.

Dedicated actions have to be taken in order to stimulate better understanding and cooperation between system research, design and process development to close the gap between complex systems and nano-device physics and technology. This should include dedicated and significantly funded programs (through dedicated calls) along with networked centres of excellence and dedicated workshops or conferences.

Domain 'Design Methods and Tools'

Rationale

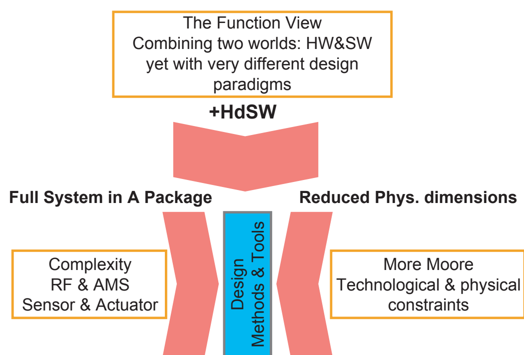
Historically Europe has a strong position in the design of complex systems, and increasingly, the design process itself generates the added value of the silicon products. To quote Handel Jones: 'IC vendors that are strong in design are generally the most profitable and are in a superior market position'. The transition from Microelectronics to the emerging world of Nanoelectronics, with 'More Moore', 'More than Moore', 'Heterogeneous Integration', and 'Beyond CMOS', will open up many opportunities for European industry. The ability to design complex products will be fundamental to capitalising on these opportunities. In this light, increased design productivity, through new methods and tools is a central theme for Europe in order for it to sustain its leading position in supplying cost-efficient silicon-based system solutions as the technology continues to transit into critical dimensions below 100 nm.

This section of the SRA describes a variety of research priorities that underpin this efficient transition, covering the time frame until 2020. The continuous shrink of device sizes within ICs and the related fabrication processes has been the foundation for the ever-more powerful integrated silicon products we all experience in our daily life. The challenges for an efficient design environment for such complex silicon products are numerous.

In the past, it was possible to isolate the design process from effects of the fabrication process such as the variability in transistor parameters. This resulted in a capable set of design tools to smoothly transform specification data into appropriate layout data that could be fed into the fabrication process, as well as enabling an appropriate verification process through the different levels of hierarchical abstraction. This process cannot be handled informally anymore. Moving to nano-scale technologies not only results in all the design steps, from specification down to fabrication, become seriously interdependent. It also results in them being intimately linked to yield and reliability.

Future design environments will have to cope with a number of major challenges. There will be a large impact from 'More than Moore', through the functional, topological and technical complexity of extremely integrated and heavily compacted systems in terms of their diversified hardware (sensors, actuators, MEMS), logic and analog/mixed-signal functionality, and their RF properties. In addition, future design environments will be impacted by 'More Moore' side effects, notably the ever-more serious fabrication and cost constraints associated with continuous downscaling of CMOS technologies and increasing process variability. The whole situation is seriously aggravated by the fact that software now has to be taken into account as part of the integrated design process. This particularly holds true for hardware design, where dependent software must be tightly coupled to the corresponding hardware in order to supply the specified functionality. Furthermore, software design-tool productivity is currently only doubling every five years, yet the market calls for it to double every ten months. This increases the already well-known hardware design-gap [5,6].

It is inevitable that software must now become part of the traditionally hardware-centric SoC integration/verification process. Efficiently combining HW and the corresponding hardware dependent software design is already a big challenge and tools to support this at lower levels are available. However, increased system complexity, which typically includes elements of mechanics, hydraulics, chemistry, magnetics and (bio)sensors, together with the trend towards multi-processor, defect-tolerant and power-managed implementation architectures, represents a much bigger challenge to which no applicable models, metho¬dologies, or tools exist today.



The design challenge in the nanoelectronics era

In order to boost design productivity, the engineering process must move to higher levels of abstraction and also consider early verification of application requirements, easy integration of new functionalities, and provision for fabrication and reliability constraints

A consequence of this evolution is that Electronic Design Automation (EDA) will play a key enabling role for Europe's future capability to cost efficiently link application requirements derived from societal and market needs with their eventual implementation in the form of compact systems in the 'More Moore', 'More than Moore' and 'Heterogeneous Integration' domains.
In this context, the availability of a superior design environment, i.e. Design Methods and Tools, is absolutely vital for Europe to sustain a leading position, not only in delivering outstanding silicon solutions but doing so at competitive design costs. To be achieved at a level of adequate performance, this will require strong and coherent activity from all major European stakeholders, guided by a roadmap with a clearly expressed vision, leading to clearly identified research priorities. It is evident that EDA vendors have a somewhat limited motivation to develop and supply advanced extensions on their own, so such a roadmap will also guide them to make appropriate investments.

ARTEMIS and ENIAC complementarities

According to the challenges described above, any design method needs to address hardware and software, individual components and the overall system, and interfaces with heterogeneous components (e.g. MEMS). Together, the ENIAC and ARTEMIS platforms address these continuums and enable continuity from application software down to silicon. To this end, they are committed to working in concert. ENIAC provides a coherent integration path for the application software and the corresponding hardware dependent software (HdSW) enabling implementation of the hardware's target functionality and the running of application software of the final hardware platform. This continuous flow will bring to the system industry three key benefits by enabling:

- Faster time-to-market thanks to concurrent design of both hardware and embedded software;
- Cost-effective design choices when building complex systems thanks to better architecture exploration at system level (e.g. different partitioning and component selection) and at implementation level (e.g. different organization to achieve different performances requirements);
- The design of more complex systems with increased reliability and improved quality of service thanks to modular design of hardware and software components.

Research Priorities

Design methodologies and modular design flow

Another revolutionary step will be a Modular Design-Flow based on a framework and a unified Design Database with a standardised Application Programming Interface (API) to communicate with any tool that may be integrated into a particular user's design-flow. Consequently, any tool fitting to this framework will

have to support this API. Such a modular design-flow would offer an enormous benefit for users, allowing them to customise their design-flow in accordance to their particular needs. Such a unified framework would also work as a powerful door-opener for European based tool vendors, by lowering the technical barriers to engagement in existing tool-flows.

The current trend towards Compact Systems such as System-in-Package (as explained in the Heterogeneous Integration domain section) requires extension of the classical SoC-centric design flow to efficiently support the More than Moore (MtM) domain. This domain is, by definition, extremely diverse. To design compact systems in the MtM domain, a MtM integration platform will be required, which can serve as a 'virtual prototyping' environment.

Priorities until 2013

- Hardware/Software Co-Design
- Transaction level modelling
- Metrics to measure and improve design pro ductivity
- Requirement mapping and engineering
- Model-based system specification
- Coherent integration/implementation of hardware and HdSW
- An integration platform for More than Moore including Heterogeneous Integration
- Integration of Design for Yield, Design for Manufacturability and Design for Test & Analysis

Priorities from 2013 to 2020

- Metrics and cost functions for the designprocess

Advanced Architectures

With respect to new chip architectures in the context of Nanoelectronics, R&D is mainly driven by two basic challenges, namely how to efficiently manage enormous complexity, and how to overcome the huge None-Recurring-Engineering (NRE) costs of future nanoelectronic SoCs.

Current approaches to address complexity are mainly characterized by multi-core solutions in connection with Networks-on-Chip (NoC). In order to design these new architectures, new methods and tools will become necessary, for performance analysis, for synthesis of multi-core architectures and NoC, and for appropriate SW coding.

All today's research activities to solve the NRE issue envisage a standard architecture combined with some kind of reconfigurability. However, no promising solution is apparent yet. This deficiency might eventually impose serious constraints on which kind of architectural approaches can cost efficiently be fabricated.

An emerging challenge is the integration of MtM concepts into this 'More Moore' architecture evolution. In addition, the design process must take into account self-configuration with adaptable components and flexible interfaces, as well as the flexible interconnection of heterogeneous components.

A longer-term priority is the design and evaluation of fault-tolerant architectures. All the 'Beyond CMOS' architectures currently being investigated are highly parallel and at the same time highly unreliable, thus needing redundant communication and computation.

Priorities until 2013

- Modelling and optimisation of Network-on-Chip architectures
- Modelling and evaluation of Multi-Core-Architectures
- Reconfigurable systems
- Development and evaluation of innovative communication concepts
- Self-adapting architectures for application-spe cific requirements

Priorities from 2013 to 2020

- Systems and architectures for fault-tolerant hardware and software
- Integration of different communication and data transmission methods in the design process
- Constraint-driven automatic partitioning

Reliability

Reliability is becoming more and more a key issue for the competitiveness of semiconductor products. As people assume high performance for their products, some application areas demand the highest levels of reliability - for example, reliability in safety-critical automotive applications is mandatory to save life and mishap on the roads. Unfortunately, the ongoing downscaling of semiconductor technologies aggravates the design of highly reliable integrated circuits, because decreasing component dimensions such as oxide thicknesses or wire diameters have a negative influence on ageing. They cause accelerated wear out of important reliability parameters in integrated circuits such as thermal behaviour, breakdown voltages, electromigration and device matching.

In principle two strategies can be approached to reach the needed reliability, being the avoidance of defects (zero-defect), and the identification and substitution of defective parts during operation (redundancy). Zero-defect requires a complete knowledge of ageing mechanisms within the circuits, enabling the modelling and simulation of the reliability gradient during operational life. Redundancy requires methods of estimating the number of expected failures, identifying defective parts and paths, and substituting them by new ones. For both approaches, however, today's tedious and expensive experimental reliability tests on processed silicon must, as far as possible, be substituted by intensive simulation methods.

Priorities until 2013

- Metrics for robustness and reliability in the design process
- Exploration of physical and aging effects at system level
- Developing redundancy at different levels
- Design for redundant hardware tolerating runtime failures
- Exploration of physical and aging effects for deep submicron technologies and new functional devices
- Design for reliability in mixed-signal and RF circuits

Priorities from 2013 to 2020

- Reliability sign-off
- Self-adaptation and self-repair

IP-ReUse

Looking to the history of design productivity, the strongest step on record was gained by the very first introduction of an automated IP reuse, i.e. 'semi-custom'. This methodology opened the door for 'cell-based design' and for subsequent RT based synthesis - a quantum leap in design productivity. What's more, it paved the way for the fruitful evolution of EDA tools and the related industry over the past 20 years. IP-ReUse was and continues to be a lasting source of ongoing improvements in design productivity.

Priorities until 2013

- Technology independent IP-transfer
- Standards to describe IPs as well as plug-intools for IP interfacing and IP packaging
- Concepts for automatic integration of IPs in on-chip networks
- Comprehensive processes for the integration of IP modules from different suppliers
- Heterogeneous multi-core architectures including software

Priorities from 2013 to 2020

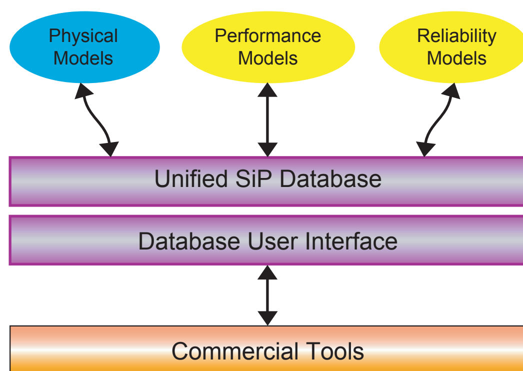
- Black box and grey box verification of IPs at the system level
- Strategies for automatic verification of IP integration

Modelling and verification

Modelling and verification continue to being of fundamental importance in an efficient design process. They account for more than 50% of the overall design costs. By allowing virtual prototyping, they are indispensable as a means of detecting design errors as early as possible in the design cycle.

Mastering increasing complexity and taking into account the integration of 'More than Moore' components in the verification process is a major challenge, certainly taking into account the increasing importance of software for

the entire chip design process. The drawback of complexity must be overcome by introducing higher levels of abstraction in combination with IP-ReUse - e.g. by moving to Transaction Level Modelling (TLM) as the next level after Register Transfer Level (RTL). Moving even further will reduce significantly the modelling and verification complexity and together with the related simulation effort.



Unified physical models integrated into the Heterogeneous Integration design-flow

To support Heterogeneous Integration (HI) and the associated Compact Systems, appropriate simulation and reliability models are needed. In addition, extended hardware complexity has to be contained by physical models that enable the creation of unified databases.

Priorities until 2013

- Modelling of real time operating systems
- Performance evaluation of hardware-dependent software
- Modelling and simulation of heterogeneous systems
- Formal specification and verification of non-functional properties
- Assertion based verification of analogue and mixed-signal circuits
- Efficient system verification for correct inter operability between digital, mixed signal, and RF chips
- Design and verification methods for hardware-dependent software and their synchronisation with the hardware design process

Priorities from 2013 to 2020

- Property checking at system and architecture level
- Simulation, emulation, and debugging at system and architecture level

Radio-Frequency/Analog-Mixed-Signal (RF/AMS)

The entire spectrum of design, combining analog, mixed-signal and high frequency domains is summarised as RF/AMS. Regardless of the ongoing 'digitalisation' that is taking place in the world of electronics, analog circuits continue to be an indispensable part of most electronic systems. With respect to design efficiency, AMS is currently lagging significantly behind digital design due to its still weak EDA coverage. Severe deficiencies exist both in the implementation and the verification path. This includes automated generation of behavioural models, automated transitions between different levels of abstraction, circuit libraries, constraint handling during the design process to enable circuit synthesis, and formal verification methods for application at various stages in the design process to supplement simulation.

All these challenges are even more difficult for RF-CMOS, a domain that is rapidly emerging as a result of the enhanced high frequency performance of CMOS technology at the 65-nm node and beyond.

Priorities until 2013

- Transformation of parameters and constraints from lower to higher level of abstraction, leading to automated abstraction
- Automated generation of behavioural models for AMS and complex RF circuits
- Technology migration for analogue circuits
- Modelling of analog and RF circuits including process and environment tolerances
- Extended RF models with high dynamic range
- Automated RF floor planning
- Complete verification flows for analog and RF circuits with constraints management

Priorities from 2013 to 2020

- Topology-based technology-independent design of RF/analogue modules

- Redundancy based reliability for RF/AMS circuits
- One pass synthesis of RF and AMS circuits

Design for Manufacturability

It is well recognised that Design-for-Manufacturability (DfM) has to be addressed within the design process for today's integrated components. However, moving further down the road of nano-scale technologies, this issue is not only is becoming more severe due to the higher impact of physical constraints. It is also becoming more severe because integrated components and Compact Systems are becoming extremely complex and extremely diverse with respect to new functionalities. As a result, any approach that address DfM within a design flow has to cover a very broad perspective. This holds true horizontally - in terms of the increasing number of specific influencing factors and extended methodologies introduced - as well as vertically in terms of an appropriate representation of all those methodologies at all levels of abstraction within a design-flow that is substantially extended towards system-level. The new functionalities in future Compact Systems require totally new strategies concerning Design-for-Test (DfT). The emerging fabless business models for IC companies in the More Moore domain definitely require innovative approaches concerning Design for Analysis (DfA) on top of classical DfT.

Priorities until 2013

- Design centring and yield optimisation
- Extraction and modelling of DfM-based layout constraints
- Modelling of variability
- Efficient strategies concerning Design-for-Analysis (DfA)
- Optimisation of the placement and layout of active and passive elements to improve yield, performance, and power consumption
- Yield-aware design process and sign-off
- Test strategies for Compact Systems comprising new functionalities

Priorities from 2013 to 2020

- Integration of Design-for-Yield, Design-for-Analysis, and Design-for-Reliability at all levels of abstraction

Ultra Low Power

Besides cost-efficiency, reduced energy consumption is going to be a key driver in all application domains. It not only defines crucial parameters such as operating and standby times for battery powered equipment, battery form factor and lifetime and electromagnetic pollution. It also creates new opportunities in applications such as eHealth, mobile devices and sensor networks. In addition, low power will be a prerequisite to broadly enable less developed countries to participate in these possibilities.

Priorities until 2013

- Dynamic Voltage & Frequency Scaling
- Optimisation of static power
- Efficient simulation of power consumption at system level
- Power management at system level including the operating system
- Leakage optimisation

Priorities from 2013 to 2020

- Dynamic power and temperature management at all level of abstraction in SoC design

Implementation

It is worth noting that EDA has a traditional association with Si-Design tools. However, here it has a new and wider context. The existing EDA solution providers are unlikely to be the providers of monolithic EDA solutions for the new era. They will have to come to terms with the fact that their role will be component suppliers within a wider New-EDA capability. The establishment of a framework for this, and the provision of tools to connect into the framework is a big opportunity for European Method/Tool providers, which are mainly SMEs.

To stimulate the Nanoelectronics industry in Europe, joint ventures between EDA suppliers, the EDA user industry and research institutes must be reinforced. Funding for EDA research should provide the platform for joint ventures, generating incentives for globally active companies to establish a culture of co-operation and conduct new developments in Europe. Finally, there must be a willingness to share the research risk. Unless

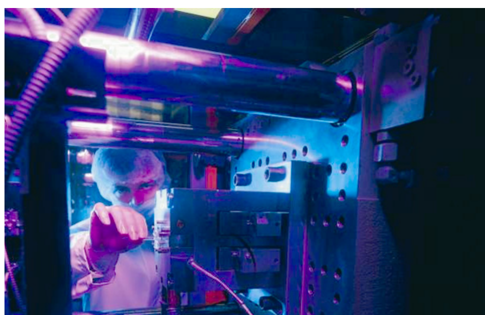
this succeeds, users will suffer as a result of being provided with EDA tools too late. As a consequence, they will not be able to optimally exploit the latest technologies, ultimately leading to degradation of the Nanoelectronics industry in Europe.

Closing the design gap is going to become a vital step in winning the system solutions race against global competition. To achieve this objective, the industrial association AENEAS is promoting co-ordinated activity between the major stakeholders in all three EDA domains -suppliers, users and research institutes.

Domain 'Equipment and Materials'

Rationale

Equipment companies exist in all shapes and sizes, from global companies offering a full spectrum of equipment, to small niche companies with very specific products or know-how. While the first group has the capabilities to make integrated products that drive down cost-of-ownership for device makers, the latter group has the agility to bring innovative products to the market fast. Although only a few companies make final equipment, these companies are supplied with subsystems and components by a large number of suppliers, each with its own part to play in the overall jigsaw puzzle. This is made possible through the many regional networks and competence centres, and the historical existence of specialised industries.



Inside nanoelectronics manufacturing equipment

The materials market is quite distinct from the equipment supplier market. It requires huge investments, and the materials science and manufacturing know-how often exists only in a small set of companies with leading-edge positions and captive markets. Although they are typically global companies, many have core R&D centres in Europe. In addition to established players, there are also newcomers with unique new products that have enabled the industry to achieve its goals more efficiently.

Both groups, equipment and materials suppliers, have one common denominator - they need to collaborate with nanoelectronics device makers and with each other to align the characteristics of their products, and to efficiently cope with the rapid pace of change that the nanoelectronics industry is experiencing.

Research priorities

Substrate Materials

Many companies are reluctant to invest in 450-mm wafers, as this requires high investment and significant resources. However, deciding when to migrate is a key decision, because more than eight years of development time is needed between preliminary research and volume production on a new wafer size. In order to make the move feasible for the European semiconductor industry and prepare the migration, a consortium of all the different semiconductor industry players is needed.

Regardless of wafer size, constant improvements need to be made at the substrate level to accompany the constant shrinkage of device dimensions. Of particular interest is the development of CZ crystal ingots/wafers with optimised defect properties. This could be achieved by new pulling processes and/or additional heat treatment during wafer manufacturing to allow optimisation of defect sizes and densities, and controlled clustering. The development of suitable internal gettering capabilities for Si wafers is key to supporting the device industry in avoiding metal-induced failures in future Low Thermal Budget processes. Special focus also has to be put on improvements in wafer parameters such as flatness, control of edge area, nano-topography and the systematic reduction of particle size and density, as well as residual surface impurity.

Volume production of thin Silicon-on-Insulator (SOI) already addresses partially depleted (PD) MOSFET architectures. The Si thickness ranges, according to design rules and applications, between 100 nm and 35 nm. For fully depleted device architectures, the layer thicknesses targeted lie between 15 nm and 30 nm. Current development of thin SOI focuses on thinner top Si layers, on improving the surface roughness to minimise local thickness variations for sub 65-nm devices, on tighter layer thickness control, and on wafer edge roll-off to further reduce the impact of SOI edge exclusion.

Silicon mono-crystal

Standard SOI substrates developed for PD SOI technologies are only the first of several generations of advanced substrates. The layer transfer technique makes it possible to create a fully engineered substrate, tailored to the requirements of an application by properly choosing the active layer, the buried dielectric and the base substrate.

Starting from an SOI wafer, there is an evolution from Si (100) as the active layer towards Si (110) and strained Si to provide mobility enhancing substrates. The mainstream choice for the buried dielectric is thermal oxide but work is ongoing to evaluate the use of alternative dielectrics or buried multi-layers for improved thermal conductivity and reduction of hot spots in the top IC layer. Furthermore, deposited dielectrics open up the possibility of including buried patterns in the dielectric layer.

The high mobility of charge carriers in Germanium makes this material well suited for sub 32-nm nodes, where it can even provide improved performance compared to strained silicon. The introduction of high-k dielectrics is an additional incentive to change the channel material itself, and makes Si loose its one major advantage over Ge - its stable native oxide. GOI (germanium-on-insulator) substrates are well suited for the integration of optical and electronic functionalities, because of the optical properties of Ge and its good lattice match with GaAs.

Device processing and chemicals

Historically, (poly)-silicon, silicon dioxide, silicon nitride and aluminium have been the materials of choice for semiconductor devices. In the last decade, however, it has proven impossible to further extend dimensional scaling with this set of materials alone. A multitude of new high-performance materials with specially engineered electrical, mechanical and chemical properties must be introduced to extend Moore's Law and allow fabrication of scaled devices that operate at higher speed and/or lower power. A huge material science effort is required to deliver the necessary properties, involving the selection, demonstration and integration of appropriate chemistries. For materials processing, established processes such as Chemical Vapour Deposition and Physical Vapour Deposition are now being complemented by processes such as Atomic Layer Deposition, electro-plating and selective deposition processes for silicon and other materials. New etching chemistries also need to be developed for the many new elements that will be introduced into semiconductor manufacturing. However, special attention needs to be given to the avoidance of toxic products or, if they must be used, to minimising the quantities required.

The parallel development of heterogeneous devices is also fuelling the demand for new high-performance materials and processes. More recent developments rely on the elaboration of nano-materials and control of the processing of mostly unexplored chemistries.

Requirements on the processing technologies needed to generate new devices as described in other domains

in this SRA will be increasingly demanding. These requirements can be outlined for the extension of CMOS technology along the following five guidelines.

Lower processing thermal budget

The increasing number of process steps and the shorter diffusion lengths in devices imply ever-lower process temperatures. Novel (metal-organic) precursors and improved equipment to introduce them in the reaction environment have to be developed. In addition, non-thermal activation by, for example, photons or radicals, will increasingly be deployed in processes. This calls for novel cleaning and treatment technologies, deploying novel chemistries and/or non-thermal activation with photons or radicals. In order to control contamination it is also necessary to increase the bulk and surface purity of the ceramics that are more and more used in process equipment.

Wafer sorter

Higher aspect ratio step coverage

Different domains will require deposition/etch technologies that have more demanding step-coverage control, or technologies that result in improved planarity. For some applications, conformal deposition is required, while for others directional deposition is required. Further development of technology platforms and chemistries for conformal deposition and removal is needed. Catalytic, super-conformal technologies in dry or wet environments and selective deposition technologies will have to be developed to preferentially fill narrow structures. A next step is the development of 3D-related photolithography e.g. for producing the DRIE masks used for 'hole-drilling' in a TSV (Through Silicon Via) process in combination with a 'Via Spray Coater'. This coating method will greatly reduce the wastage of resist material. Related to this, it will also be necessary to find solutions for handling very thin wafers, including on-carrier fixation and de-lamination.

Film interface control

Cleanliness and precise atomic-level control of interfaces will become very important. New and improved cleaning and priming technologies, in-situ interfacial measurement and control techniques, and improved control of wafer environments and logistics must be developed for all process technologies. The ability to alter micro-surfaces by applying ultra-thin conformal films has possibilities in a wide range of application areas, including microfluidics, bio-sciences, drug delivery and measurement, mechanical sensors, optics, displays, and many others.

Novel material properties

The range of accessible thin film materials, both for mainstream and special applications, will have to be expanded. New technology platforms to deposit multiphase materials such as controlled nano-porosity materials and nano-laminates, bio-materials and self-assembly layers must be developed.

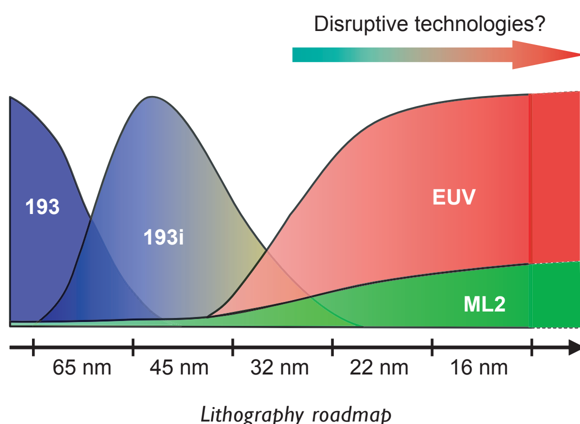
Flexible technology platforms

Flexible deposition platforms allow rapid development and deployment of new materials to pilot line maturity. Increased deployment of a wide variety of new chemicals calls for improved Environmental Safety and Health procedures to allow for the timely development of abatement and recycling technologies, plus shipping and handling procedures, so that new chemicals can be deployed quickly without any adverse impact on the environment. New devices and computational principles emerging from research rely basically on barely explored supra-molecular chemistries. Elucidation of the functional mechanisms, demonstration of the molecular fabrication feasibilities and development of the considered computation algorithms and their realisation opens up huge opportunities for research in chemical and physical principles.

Classic optical and EUV lithography

Optical lithography has been the engine of continuous scaling in nanoelectronics, and in the near future will be extended to Extreme Ultra-Violet Lithography (EUVL) - the last optical technology currently foreseen. Hyper Numeric Aperture immersion technology with fluids of high refractive index addressing the 45-nm and 32-nm nodes will be pursued. EUVL should then be pursued to the limit of its capabilities, now estimated to be at the 13-nm or 8-nm node. It is possible to extend the roadmap further by using lithography with 4 - 7 nm light, achieving almost real atomic scale imaging. Basic research to determine the best light source and mirror combination must be investigated to assess the possibilities and limits of this technology.

Optical and EUV lithography may be the key for high volume miniaturisation, but it involves very expensive tools and masks. In particular, the zero-defect requirement for masks makes them very expensive. This requires a continuation of research into exposure equipment, resists, masks and their corresponding materials and equipment and into metrology equipment for critical dimension measurement, overlay control and defect inspection, and AMC (Airborne Molecular Contamination) measurement. An additional element could be the use of optical simulations for better effect prediction and improved corrections in optical metrology on masks and wafers.



Lithography roadmap

Mask-blank suppliers need to do research into optical and EUV lithography requirements. However, extensions of optical lithography will probably reach their limit at the 22-nm node if not before, which will impose implementation of EUVL on the whole industry. This will shift the focus from defect-free masks to defect free mask-blanks, since multi-layer defects will be difficult or impossible to repair. Additionally the uniformity requirements for future nodes require sophisticated deposition tools, which combine low defect levels with very high uniformities. This will require defect suppression techniques for advanced mask production, i.e. methods and technologies for detection and removal of defects (such as particles and contaminants) that are smaller then 30 nm on structured mask substrates.

Double patterning/exposure lithography is expected to be introduced for the 45/32-nm generations to extend lithography an additional generation without the need to change to 193-nm laser light sources or develop new immersion materials. Double patterning demands much tighter tolerances for mask placement and critical dimensions, which in turn poses significant challenges for mask inspection/metrology. Double patterning will also require special measurements on the wafer to assess how well the two passes line up. These challenges must be addressed urgently if Europe is to become a leading player in this market.

A next step will be self-correction materials/structures or self-aligning chemistries for the processing of advanced lithographic masks, i.e. self-aligning fluids and self-assembly layers. Compensation of the imperfectness of materials and processes will be eliminated by self-organisation methods on mask materials/structures, with the overall goal of achieving a 'perfect' lithographic mask. Last but not least, with the introduction of these advanced techniques, accuracy is becoming even more important, which requires ultra-accurate motion systems for silicon wafer and lithography mask translation.

Mask-Less Lithography (ML2)

Apart from the 'classic' lithography that uses masks for patterning, several new ways of patterning a surface can be envisaged, such as nano-imprint lithography, and direct write single- or multi-beam lithography. Although classical lithography will remain dominant for the fore-

seeable future, it is the new technologies that could give Europe also a leading edge in more specialised niche products and markets, typically in the 'More than Moore' domain. The newly emerging mask-less lithography (ML2) has a number of advantages compared to optical or EUV lithography, in particular the lower setup cost that result from the lack of masks and simpler process.

Nano-imprint lithography (NIL) receives considerable attention since it represents the smallest replication technology currently known. Problems to be resolved include overlay capability, throughput, stamp life, stamp mastering and non-homogeneity in the polymer residue thickness and defect control. However nano-imprinting lithography has potentially low cost and high throughput for functionalised materials and for 3-dimensional patterning. An interesting application for NIL would be the development of a tool based on a classical Mask Aligner type machine that would provide wafer-scale UV cold embossing lithography. 'Nano-lawn' contacts could be used for bond pads in temperature-sensitive devices since they show considerable potential to allow lower bonding temperatures.

Recent developments in Multi-Beam Technology (MBT) have proven that this technology could become well suited in the medium term for small and mid-sized production volumes, reducing although not eliminating its throughput handicap, even for small feature sizes. As basic knowledge has been gathered, efforts must be made to build prototypes and create an equipment manufacturing base in Europe for this technology. It is probable that only massively parallel e-beam systems delivering the highest resolution in each beam will be able to solve the challenges for technology nodes smaller than 45 nm.

Metrology

Metrology is one of the strongholds of SME equipment manufacturers in Europe. It consists of highly specialised companies with unique capabilities. Although metrology has been regarded as 'trouble' in a production line, it is essential to achieving short learning curves for yield improvement and for reducing debug costs. As metrology techniques become faster and less expensive, there is a trend towards increasing the number of in-line metrology points.

Mask inspection, metrology, and repair

The goal of photo mask quality control should be to detect defect growth at a point where any defects are just beginning to form but are not yet yield-limiting. A carefully developed mask re-qualification inspection strategy should be implemented to optimise mean time to failure. However a major problem for the industry is real-time line-width measurement below 10 nm. Of the various techniques currently available, Scanning Proximity Probes are the most appropriate in terms of accuracy and ease of measurement. However, the technique needs to be urgently enhanced to enable high-speed imaging. The ability to perform high-speed in-line metrology at these dimensions will put the European semiconductor industry in a world leading position.

Mitigating defects either by in-situ repair or by actively preventing defect generation and defect migration will probably not be enough. In-situ and ex-situ measurement techniques will be required to differentiate between defects that print, defects that do not print and false defects that result from measurement but have no influence on the blank performance. Particle surface interactions will play a key role and need to be investigated together with cleaning and repair methods.

Further developments in mask repair are necessary to avoid charging effects and to improve the throughput and metrology limitations.

In-line defect inspection

Because killer defects scale with the device, new technologies need to be developed into products in order to maintain high yield levels. These capabilities include:

- A new nano-defects inspection platform with tens of GHz pixel-rate to enable production worthy throughputs by adopting major advances in multi-beam technology for detection purposes;
- A new shorter wavelength light source for optical inspection in order to see smaller defects;
- New imaging technologies, suitable for nm-regime

in-line non-destructive imaging for review and classi fication purposes;
- R&D into process technologies for sub 32-nm nodes requires advanced measurement capabilities that do not at present exist. Advanced technologies for metrology then need to be developed for industrial applications.

Activities where breakthrough improvements for future technology nodes are required include:
- Quantitative Impurity/Dopant profiling with sub-nm spatial and depth resolution with 3D-capabilities;
- Carrier/resistivity profiling, as the introduction of advanced implants and annealing processes has led to significant differences between dopant profiles and active carrier levels, which imposes new requirements for probing active carrier levels;
- Compositional analysis, because many thin layers require new methods to probe their composition with high quantification accuracy, sub-nm depth resolution for analysing the dominant influence of interfacial composition, high spatial resolution (nm), and information on the chemical bond structure;
- Structural analysis because novel device structure concepts, such as strain in transistor channels, sidewalls and CNT-contacts, require probing of the crystalline nature of very thin films with very high spatial resolution;
- Development of methods for new defect types such as surface roughness, buried defects, voids, leakage sources, mobility enhancement, immersion defects;
- Enhanced imaging techniques, e.g. spectral techniques;
- Development of application-specific cameras with dedicated signal processing capabilities;
- Integration of new devices design, inspection and metrology to automate DfM (Design for Manufacturability), through the development of automatic recipe generation solutions, defect classification techniques using design data, and fast automated inspection technologies;
- Development of metrology solutions for new device structures, such as multi-gate transistors, nanodots, ultra high aspect ratios, new spacers and other novel structures.

Extremely small feature inspection

The measurement and diagnostics of shrinking features has become significantly more important and more challenging. Where optical technologies were once sufficient to see minimum features, the industry now uses scanning electron microscope (SEM) technology. However, in the next few years we expect to reach the resolution limits of SEM. As a result, it is now critical to develop solutions beyond this limit. Contamination of wafers during SEM measurement and review has become critical as dimensions shrink, to the extent that contamination threatens to prevent sampling of some layers in SEM. This can only be resolved by the use of advanced vacuum chambers. Similarly, charging, resist deformation and other effects during SEM exposure must also be addressed to meet next generation requirements.

Related to this, it is recognised that the other domains rapidly increase the diversity of minimum feature structures and materials. This complexity poses more and more challenges for measurement and imaging which must be addressed in order to provide leading-edge tools.

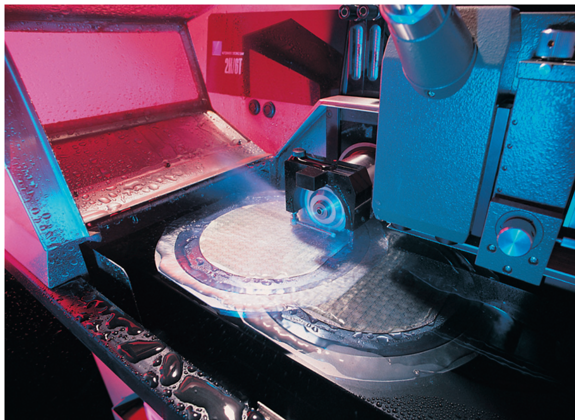
Packaging and final testing

Many packages are application-driven, always requiring smaller size, better heat transport, lower cost, etc. Traditional carriers for chip devices, such as lead frames and substrates, will be eventually replaced by novel fine-pitch developments. Nevertheless, the chip will still have to be protected from the environment. Research should focus on areas such as the encapsulation of sensor/MEMS wafers with free contact pads and free sensing areas. Technology, encapsulation materials and equipment have to be developed for these applications.

Thin wafers will be used more and more in micro/nanoelectronic equipment of the future. The handling of such wafers and substrates in probers is not yet solved. The development of a thin wafer handling system, dedicated for passivated substrates, suitable for testing in a fully automatic probe station will be required within the next few years.

Driven by strong miniaturisation, and the strong need for density increases at packaging level, new techniques like wafer-level packaging and 3D packaging will find their way into new products. Many improvements need to be developed, such as better through-substrate vias for thinned dies and wafers, and better materials to fill the via holes. Europe has a significant knowledge base on laser tooling that enables vias smaller than 25 nm. Equivalent technology is also used for dicing, allowing for less kerf-loss and higher design flexibility.

Testing within economical limits is becoming a critical issue in advanced device manufacturing. Techniques such as DfM and DfT are essential to managing the complexity of hybrid systems. In this area there is the need to develop new approaches, through a combination of hardware and design solutions. The wide range of requirements will offer plenty of space for innovative solutions and for the rise of high-tech SMEs.



Wafer sawing

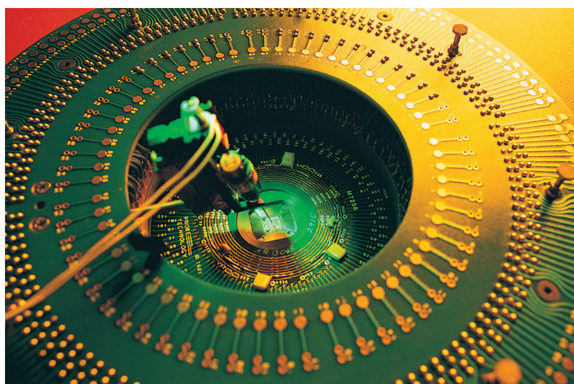
Implementation

Of the total world-wide market for equipment and materials for the semiconductor industry about 9% was created in Europe. The equipment market is slightly larger then the materials market. Because the industry is highly globalised, it is strongly influenced by global trends, particularly the dilution of manufacturing capacity towards other continents. Nevertheless, this dilution is not as strong as it could be, because equipment and materials manufacturing requires high levels of expert knowledge and experience, which are difficult to relocate. This is of high value to Europe, because additional future investment in this segment will result in the slowing down, and eventually reversing, of this trend. It will ensure that Europe remains a world leader in highly specialised segments such as lithography, MEMS and others technologies. Maintaining these leading positions is key to maintaining the attractiveness of Europe as a region for nanoelectronics industry investment. This can be achieved by the collaborations described below.

Research collaborations are often based on the critical phase of prototyping new equipment or material with a lead customer or lead customers. Three models exist. The first of these takes the form of technology platforms in which material suppliers and equipment manufacturers embody their newest developments, and on top of which research teams in institutes and industry evaluate and improve the technology. The second model is where a prototype is made for a specific user as a beta-test platform, typically with the help of key component and material suppliers. In the third model, universities also undertake collaborative research projects with an equipment manufacturer or material supplier to remove technology hurdles, and through basic research explore the possibilities for future technology breakthroughs. The first model requires significant resources, and as such, only a few institutes can offer this service. The second model is often used by spin-offs that need to win market acceptance. The third model is often used by industry as the seeding ground for potential new products, and often takes the form of project based bilateral research in which all know-how belongs to the industrial partner.

There is also strong collaboration between the larger equipment suppliers and the equipment component manufacturers in Europe, that creates a flexible knowledge community around the main supplier. This enables SMEs to provide highly specialised products to the nanoelectronics industry, while also supporting other industries, such as the food, medical or automotive industries. This creates a spill-over effect to other industries, strengthening the overall industrial network of Europe. Device makers also work with SMEs, but

SMEs often experience hurdles to becoming an accredited supplier of these larger companies. In this respect, research networks and other platforms are often essential for SMEs to get on the radar screens of the large corporations.



Micro-wiring

Both in research and in manufacturing consortia, private-public partnerships are essential in order to create an environment where different companies can approach each other, and investigate the possibility of stronger collaborations at reasonable levels of risk. Through the creation of such public-private partnerships, optimal conditions are created for the next-generation products and technologies that will guarantee Europe retains critical know-how in this high-tech industry. In order to achieve this, a simple, transparent and efficient project proposal and evaluation process is essential, so that a minimum of resources is used in a phase where there are no guarantees of project acceptance. In addition, the lead-time for project approval must be short, because windows of opportunity are often small. The present FP7 model of calls for specific topics is not efficient for SMEs, as it is often not matched with the short- to mid-term research needs typical in the Equipment and Materials domain.

Conclusion

In a world where Moore's Law and advanced CMOS process technologies govern the integration density of digital logic and memories, major and continuous investments have to be made by all players in the value chain to keep up with the pace of innovation. For each new process technology generation, costs go up, yet at the same time market growth for the semiconductor devices produced using these next-generation processes is decelerating. The result of these conflicting trends is an ongoing process of segmentation and specialisation in the industry, with only a few players remaining globally that can provide sufficient R&D mass. In addition, new designs in these new technologies are suffering from rapidly rising non-recurring engineering (NRE) costs. Capital requirements in 'More than Moore' and 'Heterogeneous Integration' technologies tend to be relatively low compared to the needs of advanced CMOS ('More Moore'). This is because in many cases process know-how and manufacturing infrastructures inherited from past generations of CMOS manufacturing can be re-used to produce 'More than Moore' and 'Heterogeneous Integration' devices. This ability to re-use existing infrastructures may in turn limit the market for new semiconductor manufacturing equipment.

All technology domains, including 'Design Methods and Tools' and 'Beyond CMOS', have in common a growing proliferation of options and an explosive diversity of required materials. This makes it difficult for the European industry as a whole, let alone individual players, to realise sufficient critical mass in terms of initial know-how and eventual business volume. This is a major issue, not only for component manufacturers and system houses, but also for suppliers at the front-end of the value chain, as described in the 'Equipment and Materials' chapter of this SRA. These front-end companies will need to produce highly specialised materials and build new manufacturing equipment to keep the world's nanoelectronics factories running. Certainly in the 'More than Moore' and 'Beyond CMOS' domains, with their very high option diversity and initially fragmented application markets, public-private partnerships will be needed to bridge the gap between innovation and future volume markets.

As described earlier, sustainability is a strong driver for the 'Energy and environment' lead market. Sustainability is also a key factor in the business processes of nano-

electronics manufacturers in Europe. Although the physical volume of all the nanoelectronics devices produced in the coming year is hardly significant, scarce and expensive materials will be needed to produce them, and large amounts of energy and water will be required to maintain the necessary ultra-clean development and production environments. The industry is therefore very conscious of the responsibility that it carries, and far-reaching targets have been set, largely on a voluntary basis. In order to prevent unfair competition in this respect, the European governments and the EC can play an important role in making sure that other regions around the world abide to similar environmentally friendly targets.

In summary, it is evident that nanoelectronics research is conducted in an arena of multidimensional complexity, spanning everything in the development cycle from idea to realization and in the supply chain from materials science to volume manufacturing. Research centres and manufacturers therefore play key roles. In-depth know-how is needed at every stage in the process and every step of the way involves a moving target because of rapidly changing application markets. Keeping all stakeholders connected and informed is therefore extremely important to achieve and maintain a strong multidimensional value ecosystem for nanoelectronics in Europe. However, it must also be realised that the nanoelectronics business and the associated technical challenges are part of a market environment that spans the entire globe. Europe must reinvent itself to maintain and extend the leading position it enjoys in nanoelectronics today. To support the process, existing mechanisms for public-private partnership should be revisited, and new mechanisms introduced, using this SRA for guidance.

European ecosystem

Opportunities and threats

With approximately 800 million people, Europe is one of the largest consumer and industrial markets in the world, with advanced technology and efficient manufacturing capabilities. Europe represents 20% of the worldwide semiconductor components market and 10% of the related equipment and materials market, totalling about € 64 billion per annum. According to a recent inventory by the SEMI organisation, Europe accounts for 278 wafer fabs and more than 300 equipment, materials and service providers for the semiconductor and related industries [1].

Nanoelectronics is a global market that is strongly addressed by European industry and academia. Europe contains the headquarters of a significant number of top-10 multinational companies developing and manufacturing products for semiconductor markets. Health and wellness, transport and mobility, security and safety, energy and environment, communication and infotainment are application areas where Europe has world-leading positions.

There are strong links between Europe's semiconductor industry and the application industries that it serves. Both domains include a widespread network of SMEs, as in the automotive and semiconductor equipment industries, where the role of nanoelectronics innovation is substantial. In a modern car, for example, the value of embedded electronic components can be as high as 25% of the total component cost, and this percentage is still rising. SME involvement continues to evolve and grow in many European countries. It includes a steady stream of innovative start-ups and spin-offs with industrial and academic origins, made possible by a solid ecosystem of academic education in Europe that includes many universities with excellent international track records. Europe is also home to a number of world-class independent research institutes operating in the field of nanoelectronics that attract industrial research partners from all over the world.

The essential growth of R&D investments in nanoelectronics is not only a matter of money. It is also a matter of people. Both industry and academia (universities and research institutes) need a continuous supply of well-educated and entrepreneurial engineers to sustain growth in the nanoelectronics industry. Unfortunately, the number of graduates coming out of European universities today is not even enough to maintain Europe's current level of nanoelectronics R&D.

A specific issue for Europe is the fragmentation of research caused by the fact that state (national) policies often result in less than ideal conditions for the sharing of resources or ideas. Many good examples of cross-border collaboration do exist, but these interactions nearly always require very careful preparation in view of different regulatory issues and customs at almost every level. In addition, labour issues remain a continuous challenge. These range from the flexibility of the work force to the mobility of engineers and scientists, both between academia and industry and between different countries. Some of these issues could be solved by improved regulation. Others are too closely linked to the European social system to allow a solution within a reasonable timescale.

The European nanoelectronics industry has to compete on a global scale. Although creating a level playing field within the boundaries of the EU is necessary, it not sufficient. Any benchmark concerning ecosystems in this domain must be done with global competition in mind, and must particularly take into account government initiatives that locally support nanoelectronics R&D clusters in various parts of the world. These include well-established environments such as Europe and the USA, but also newly emerging high-tech regions such as China and India.

Stakeholder roles

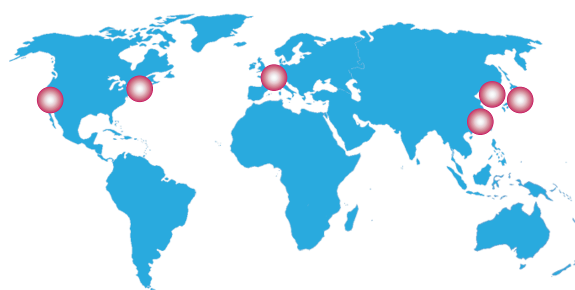
Europe's semiconductor industry is healthy, and many of

today's players are diversifying into related markets, such as solar energy. Its manufacturing infrastructure is based on a good mix of in-house manufacturing, working with alliance partners, and using foundries. Alliance partnerships are definitely still needed and provide strong added value. However, their format and the partners involved will change. Realizing that the race for pure CMOS scaling is not the ultimate goal, Europe has to look for consolidation of its industrial and academic strengths around focussed market segments.

An early product market of sufficient scale offers the potential for a higher return on investment and with that, reduced risk. Proximity and local requirements are key features of many such markets and relationships and hence influence the choice of R&D and business location. Well-organised R&D ecosystems are needed that foster parallel emerging technology developments. Such ecosystems must enable cross-fertilisation in an atmosphere of open innovation while protecting the IPR of the players involved. In the ideal ecosystem, highly innovative R&D infrastructures are situated in close proximity to traditional production methodologies. This stimulates convergence of know-how from all domains and reduces the inevitable struggle for innovative concepts to become accepted in volume applications.

Many new technology options will be generated from start-ups and innovative SMEs emerging from academic research. To bridge the inevitable gap between a good idea and commercially viable market success, such SMEs will at some point need to associate with large industry players in order to get access to volume manufacturing as well as to become sufficiently visible for leading customers. Policy measures should therefore recognise that large firms are an essential part of the innovation process. The recent trend of concentrating support mechanisms on SMEs alone ignores the natural ecology of the industry. Small firms only thrive in the slipstream of large firms (who are their key customers) and both groups wish to work within the same initiatives. Ideally, the European R&D ecosystem for nanoelectronics will be a marriage of large and small industry players - notably start-ups, together with universities and institutes. However, public authorities must also join as a committed partner, assisting in the creation of linkages between markets and technologies, building and concentrating R&D ecosystems, and securing IP leadership by implementing appropriate legislation.

Entrepreneurship is essential for effective innovation in the nanoelectronics environment. However, financial risk-taking in Europe in support of entrepreneurs is relatively weak in comparison to other leading hi-tech regions of the world. The required entrepreneurship can be stimulated in many ways, from training programs in higher education to venture capital funding for nanoelectronics-based SMEs in which finance providers, including governments, accept a significant share of the risk.



Nanoelectronics R&D ecosystems – industry, academia, authorities cooperating

Universities, research institutes and industry must extend their collaboration to make sure that Europe provides sufficient resources for R&D and innovation in business as well as in technology. In parallel, EU governments must strive to improve the structural mobility and adaptability of Europe. Because of the global nature of the nanoelectronics market, Europe needs to be able to accommodate the global mobility of the scientists and engineers that make up a virtual network connecting the worldwide industrial knowledge infrastructure. Solving this problem requires a consolidated approach from all stakeholders.

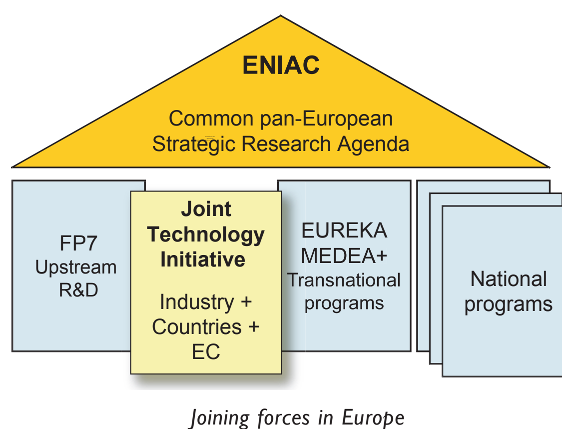
Making it happen

Mobilizing Europe

Implementing the technology domain research priorities set out in this SRA in order to enable lead markets and meet societal needs for nanoelectronics is a challenge that no single industry, knowledge institute or country can resolve on its own. A collaborative model is needed that amplifies the strengths of Europe by effectively connecting all R&D resources in the European ecosystem. This is a challenge ENIAC has in common with ARTEMIS, the embedded systems ETP. Nanoelectronics and embedded systems together support the total application area for electronic products and services, one providing the hardware and the other providing the software technology. Materialisation of these two enabling technologies into applications is facilitated through the EPoSS smart systems ETP [19].

Sharing of R&D effort through public-private partnership has proven to be very effective in establishing Europe's position in microelectronics. Today, the EUREKA cluster MEDEA+ is already driving execution of a large part of the ENIAC SRA by coordinating large transnational R&D projects [20]. Similarly, the EURIPIDES cluster covers a complementary albeit smaller segment [21]. Major research institutes have been established, such as IMEC, CEA-Leti and the Fraunhofer VmE, that today receive worldwide industrial and scientific recognition. These institutes play an important role in stimulating the research ecosystem for nanoelectronics and in developing scenarios for the future [17]. In its work package for 2007 and 2008, the EC 7th Framework Program (FP7) addresses a broad portfolio of upstream research topics derived from the first edition of the ENIAC SRA [5], such as next-generation nanoelectronics components and electronics integration and nanoscale ICT devices and systems.

Building on the networks created in these partnerships, regional competence clusters have been established that mobilize and connect local players from large-scale multinationals, SMEs, research institutes and universities on a common nanolectronics-driven agenda - for example, Silicon Saxony (D), the Pôle de Compétitivité Minalogic (F) and Point-One (NL). Inspired by the far-reaching ambitions of ENIAC, leading scientists from across Europe have organized in the form of the ENIAC Scientific Community Council (SCC) an independent body that advises and actively interacts with the ENIAC ETP in all of its activities, including the review and updating of the SRA. On the policy level, the ENIAC vision and ambition are strengthened and supported by sharing forces with the European industrial groups SEMI-Europe, ESIA, and EICTA.



Joining forces in Europe

Roadmap for partnership

The ENIAC SRA is the common envelope encompassing definition and execution of R&D in nanoelectronics in Europe for all players (industry, academia, and public authorities) and all mechanisms for public-private partnership (national, transnational, and EC). This includes many examples given in the previous section. However, despite the good work and the significant progress outlined in these examples, they remain partial solutions, only touching islands in the much larger archipelago of overall nanoelectronics challenges. Public efforts are not sufficiently aligned, and valuable time and effort are unnecessarily lost in bureaucracy.

Net R&D investment by the nanoelectronics industry in Europe was estimated to be € 3400 million in 2005, of which about 17% is executed in public-private partnerships. To realize the ambitions outlined in this SRA, the industry collaborating in ENIAC has proposed a doubling of the efforts in public-private partnerships through a joint program, with R&D investments from industry, members and associated states, and the EC adding up to € 5 billion. Such a unified approach will enable further growth of the R&D investment in nanoelectronics in Europe to € 5600 million in 2015, a level considered necessary for the European industrial and academic network to maintain its global competitiveness [5].

The ENIAC Joint Technology Initiative (JTI) proposed by the EC is a partnership model that can combine all the public and private efforts needed for resolving the R&D priorities in the SRA for nanoelectronics [22,23]. Execution of the JTI will be though a Joint Undertaking (JU). Anticipating the installation of this JU, a group of key industries cooperating within ENIAC have established the AENEAS industrial association to enable participation of all industrial and academic stakeholders actively engaged in nanoelectronics R&D in Europe. As demonstrated in a recent report issued by the AENEAS organization [24], large financial long-term commitments are required from all parties for the JTI/JU to become a success. Until that is certain, all existing mechanisms need to be examined and tuned under the umbrella of the ENIAC SRA. This includes securing the position of ENIAC in FP7, aligning with MEDEA+ and its anticipated successor CATRENE.

To provide a fertile breeding ground for R&D projects emanating from the above approach, the nanoelectronics institutes and the regional competence clusters must actively work together on strengthening the total research infrastructure in this sector together with academia in Europe and abroad. The SCC needs to address the human capital roadmap for nanoelectronics in Europe, attracting and motivating young scientists and preparing education programs that deliver new skills.

Acknowledgement

A core team of representatives from leading European industries and knowledge institutes coordinated the inputs and concluded the final text of the SRA. The members of this SRA2007 Working Group were:
Rolf Aschenbrenner (FhG). Eddy Blokken (SEMI), Michel Brillouët (CEA-LETI), Patrick Dewilde (TUD), Guy Dubois (MEDEA+), Adrian Ionescu (EPFL), Roger de Keersmaecker (IMEC), Norbert Lehner (Infineon), Mikael Ostling (KTH), Harald Pötter (FhG), Herbert Reichl (FhG), Fred van Roosmalen (NXP), Lothar Schrader (Infineon), Dominique Thomas (STM), Gilles Thomas (STM), and G.Q. Zhang (NXP).
Dedicated teams for each technology domain supported the SRA2007 working group throughout the process. Special acknowledgements go to the many people that helped to build the SRA through their contributions in these domain teams. This includes Jouni Ahopelto, Asen Asenov, Peter Ashburn, Francis Balestra, Kees Beenakker, Eric Beyne, Hermann Bittner, Bernhard Breeger, Peter Caldera, Bernard Candaele, Alain Cappy, Carlo Cognetti, Stefan de Gendt, Walter De Raedt, Andrea di Matteo, Alex Dormann, Pietro Erratico, Andreas Fischer, Olaf Fortagne, Jürgen Frosien, Roland Germann, Mart Graef, Dirk Gravesteijn, Guido Groeseneken, Leonard Hobbs, Ingo Höllein, Ahmed Jeraya, Hans-Georg Kapitza, Jörg Kiesewetter, Peter Koch, Klaus Kronlof, Rudy Lauwereins, Lode Lauwers, Bruno Michel, Laurens Molenkamp, Jean-Luc Morand, Marco Morelli, Wolfgang Müller, Valerie Nguyen, Mikael Ostling, Jenny Patterson, Ralf Plieninger, Klaus Pressel, Bernold Richerzhagen, Walter Riess, Fred Roozeboom, Wolfgang Rosenstiel, André Rouzaud, Keith Rutter, Heiner Ryssel, Enrico Sangiorgi, Jean-Pierre Schoelkopf, Marie-Noëlle Semeria, Clivia Sotomayor-Torres, Peter Stallhofer, Marc Van Munster, Peter van Staa, Co van Veen, Ton Van Weelden, Peter Vettiger, Thijs Viegers, and Peter Zegers.

References

[1] SEMI Industry Strategy Symposium Europe 2007, Zurich, February 4-6, 2007
[2] EECA-ESIA 'The European Semiconductor Industry: 2005 Competitiveness Report'
[3] European Commission, 'Creating an Innovative Europe - Report of the Independent Expert Group on R&D and innova tion appointed following the Hampton Court Summit', 2006, ISBN 92-79-00964-8
[4] European Commission, 'Vision 2020 - Nanoelectronics at the Centre of Change', 2004, ISBN 92-894-7804-7
[5] ENIAC Strategic Research Agenda, First Edition, Barcelona, November 23, 2005
[6] ENIAC Strategic Research Agenda, 2006 Update, Monte Carlo, November 30, 2006
[7] http://www.eniac.eu
[8] Michael Friedewald, Olivier Da Costa (editors), 'Science and Technology Roadmapping: Ambient Intelligence in Everyday Life', JRC/IPTS-ESTO Study, June 2003
[9] http://www.artemis-office.org
[10] Richard P. Feynman, 'There's Plenty of Room at the Bottom', Engineering & Science, Caltech, February 1960
[11] Gordon E. Moore, 'Cramming More Components onto Integrated Circuits'. Electronics 38, April 1965
[12] http://www.itrs.net
[13] http://nri.src.org/member/about/default.asp
[14] http://www.photonics21.org
[15] http://www.ist-mona.org/home.asp
[16] http://www.phoremost.org/about.cfm
[17] MEDEA+ Scientific Committee, 'Towards and Beyond 2015: Technology, Devices, Circuits and Systems', February 2007
[18] http://www.suschem.org
[19] http://www.smart-systems-integration.org/public
[20] http://www.medeaplus.org
[21] http://www.euripides-eureka.eu
[22] European Commission, 'Proposal for a Council Regulation Setting up the ENIAC Joint Undertaking', Brussels, June 22, 2007, COM(2007) 356
[23] European Commission, 'Analysis of the effects of a Joint Technology Initiative in the area of Nanoelectronics', Brussels, June 22, 2007, SEC(2007) 851
[24] 'AENEAS' response to EC roadmap for Joint Technology Initiatives', Paris, August 2, 2007

Strategic Research Agenda