

SEMICON[®] *Europa*2008

OCTOBER **07-09**

GERMANY

Stuttgart/New Stuttgart Messe

www.semiconeuropa.org



2008

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POSSIBILITIES

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for the latest agendas and details.

Welcome to SEMICON Europa 2008 in Stuttgart

Global chip sales continues to grow at about 4% for 2008. The equipment and material market in Europe is predicted to grow from \$6.2 billion this year to almost \$ 6.5 billion in 2009 (SEMI forecast consensus).



Users and suppliers are getting ready for a market rebound.

More Moore – Moore’s Law is being pushed towards limits with new tools, technologies and products to extend device scaling. New devices will require advanced equipment and new materials and substrates.

More than Moore – Advanced packaging, and MEMS, are enabling technologies, essential to new electronics applications in the automotive, mobile communications and consumer electronics industries.



Enhancing Existing Fabs – Although “New Fabs” and talk of “450mm wafers” capture the headlines, major revenues are made within existing and upgraded fabs. Fab enhancements are going on across the globe, spurring new business and growth opportunities for suppliers, and customers.

At SEMICON Europa you can explore practical solutions to enhance existing fab performance, keeping it fit for purpose and competitive.

Research & Development in Europe – Discover innovations and ‘break-through’ ideas with the most reputable European research clusters such as Fraunhofer, IMEC, CEA-LETI. These and more key institutions will share R&D projects and roadmaps providing valuable insight on industry trends and immediate business opportunities.

SEMICON Europa continues to be the premier conference and exhibition that brings together over 600 companies and over 12,000 executives, managers and technology experts. At the exhibition, technical programs, standardization meetings, and high level networking events, you will exchange views with industry partners and peers and stay on top of European and global industry aspects.

I invite you to visit SEMICON Europa 2008 and look forward to meeting you in Stuttgart!

Heinz Kundert
President
SEMI Europe

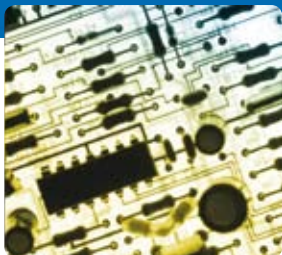
SEMICON Europa mobilizes **European strengths**

- Three days of networking
- All under one roof
- Device manufacturers, suppliers, SMEs, start-ups and R&D will be present.

SEMICON Europa facilitates **expansion into high growth markets and new technologies**

- Semiconductor (including Nanoelectronics)
- Photovoltaic
- Test, Assembly & Advanced Packaging
- MEMS/Microsystems
- Research and development





Experience

SEMICON Europa 2008

- MEET key industry players
- DISCOVER new suppliers
- PARTICIPATE in technical programs & standardization meetings

New products, Applications and Tools

SEMI Technology Arena

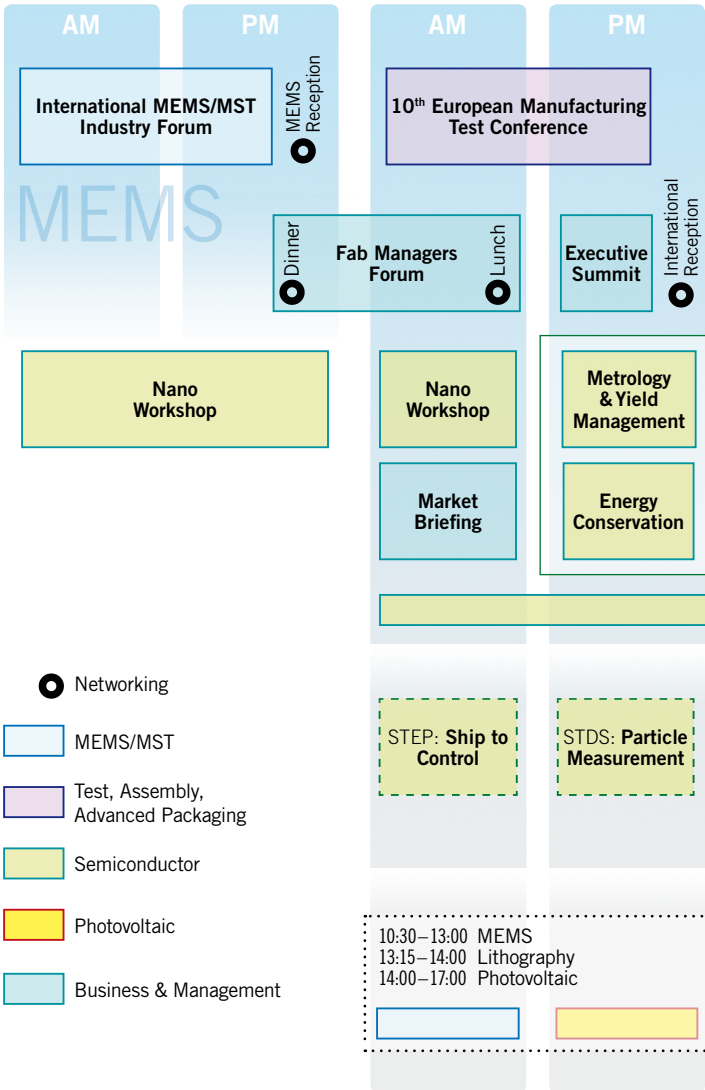
Participating companies include:

- AIS Automation
- CEA-LETI
- CSEM
- EVG
- FEI
- Fraunhofer
- FujiFilm
- Huettinger Elektronik
- IMEC
- L&T Infotech
- MicroChem
- MiPlaza
- Multitest
- MW-Zanders
- Newport
Spectra-Physics
- Philips
- Primaxx
- Ricmar
- Silicon Saxony
- STS
- Suss MicroTec
- Tescan
- Xactix

schedule at a glance

Monday 6th October

Tuesday 7th October



For detailed overview please visit www.semicon.europa.org

Wednesday 8th October

Thursday 9th October

AM

PM

AM

PM

TAP

PV

S/C

Advanced Packaging Conference

4th Photovoltaic Manufacturing Conference

"More than Moore" SC Technology

Litho/Mask Technology

Design for Manufacturing

Plastic Electronics

New Materials/ Unit Process Steps

SEMI Technology Symposium

SEMI INTERNATIONAL STANDARDS MEETINGS

SEMI INTERNATIONAL STANDARDS WORKSHOPS

STDS: 7th Si Wafer Workshop

STEP: SEMI S2/S8 Safety

STDS: IEC62061 & ISO13849 Safety of Machinery Seminar

EXHIBITION HALL1

10:30–13:00 Test/Packaging/MEMS
13:30–14:30 Automation
15:00–17:00 Refurbished Equipment

10:30–13:00 R&D Science Park Institutes
13:00–15:00 Industry Association

SEMI TECHNOLOGY ARENA – EXHIBITOR PRESENTATIONS

Parallel Event: MiNaT

Nanoelectronics Workshop – EC-Funded R&D on Characterization, Process Technology and Equipment Assessment

Monday, 6 October, 11:00–19:30

Tuesday, 7 October, 09:00–12:30

ICS—International Congress Center, Stuttgart, Germany

For the introduction of advanced technology nodes and new device architectures, proven equipment, key processes advances and process control introduced in a cost-effective manner now dictate the timing, rather than sequential lithographic scaling. Based on successful concepts that have progressively evolved in former European collaborative programs, three European funded projects like ANNA, SEA-NET and PULLNANO provide innovative approaches that speed up the development of new and advanced semiconductor nanotechnologies covering characterization, process technology and equipment assessment. In three different sessions these project will give an overview of their goals and objectives as well as provide latest results.

Session 1: ANNA

Monday, 6 October, 11:00–19:30

The European Alliance Analytical Network for Nanotech (ANNA) realizes the European strategy for improvement of existing infrastructure, for development of synergies, innovative methods in the area of metrology, analysis and characterization in micro and nanotechnologies. The infrastructure ANNA forms an independent analytical infrastructure within Europe having the expertise and competence to solve metrology problems occurring during the development of various technologies for nano and micro electronics. ANNA is an Integrated Infrastructure Initiative (I3) and focusing on the improvement of the structure of the European Research Area.

Within the project ANNA, the unique possibility of Transnational Access is offered to 18 European infrastructures

located in eight European member-states operated by universities and research institutes.

Characterization of Nanostructures

- Introduction and Overview of ANNA
Andreas Nutsch, Fraunhofer IISB
- SSRM and Atom Probe Characterization
Wilfried Vandervorst, IMEC
- Characterization of Deep Interfaces
Speaker to be confirmed
- Ultra-Shallow Junction Depth Profiling
Damiano Giubertoni, FBK
- Thin-Film Characterisation Using Ion Beam
Jaap Van Den Berg, USAL
- Applications of Surface Sensitive Techniques to Ultra-Thin Film Characterization
Spyridon Ladas, UPAT

Session II: Semiconductor Equipment Assessment for NanoElectronic Technologies (SEA-NET)

This session will introduce the integrated project SEA-NET, funded by European Commission, as well as the latest innovative results from the project. The main objective of SEA-NET is to validate emerging semiconductor manufacturing equipment for advanced process requirements at the 65 nm, 45 nm and 32 nm and 22 nm technology nodes together with the necessary advances in equipment and materials for cleaning/etch, metrology/analysis, modeling/Advanced Process Control (APC) and production control for both standard and new nano-electronic CMOS architectures. The project includes 18 semiconductor equipment assessments, several of which will be presented in more detail.

- Introduction and Overview of SEA-NET
Lothar Pfitzner, Richard Oechsner, Fraunhofer IISB
- Ruthenium Atomic Vapor Deposition AVD®, Enabling Solutions for Emerging Semiconductor Applications
Peter Baumann, Aixtron
- Low Energy and Dose Implant Test
Tibor Pavelka, Semilab
- Thermal Laser Separation Dicing System
Hans-Ulrich Zühlke, Jenoptik Automatisierungstechnik

- Pulsed Plasma Immersion Ion Planter
Laurent Roux, Ion Beam Services
- Linear Dynamic Deposition PVD
Wolfram Maass, Singulus Nanodeposition Technologies
- Sub-project on Discrete Event Simulation
Markus Pfeffer, Fraunhofer IISB

Session III: PullNano

Tuesday, 7 October, 09:00–12:30

Part 1

Advanced Physical Characterization in PULLNANO

- Strain Mapping of Layers, Nanostructures and Devices by Transmission Electron Microscopy
CEMES (speaker to be confirmed)
- Physical Characterization of Dielectrics and Interfaces
C. Wyon, CEA
- Differential Hall Characterization
N. Cowern, Newcastle University, UK

Part 2

Advanced Electrical Characterization in PULLNANO

- Scanning Capacitance Microscopy for Dopant Mapping and Oxide Characterization
CNRS (speaker to be confirmed)
- Characterization of High-K Dielectrics by Electrical SPM Techniques
M. Rommel, V. Yanev IISB, Fraunhofer
- Guidelines to Improve Mobility Performances and BTI Reliability of Advanced High-K/Metal Gate Stacks
CEA-LETI (speaker to be confirmed)
- Interface Characterization of MOS Devices
K. Souifi, INL Lyon

Who should attend

Process and equipment engineers, engineering managers, senior professionals in equipment procurement and manufacturing and fab managers from the semiconductor industry.

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€50	€80
Non-Members	€50	€80

SEMI Technology Symposium: Energy Conservation

Tuesday, 7 October, 13:30–17:00

ICS—International Congress Center, Stuttgart, Germany

Energy Conservation is a topical issue for all levels of the semiconductor industry supply chain. Suppliers and users need to jointly drive reduction in energy consumption, the ‘carbon foot print’. Leaders in the industry demand energy conservation initiatives and control systems that quantify energy and resources consumption.

How can we establish a reference; how can we identify improvement targets; and, how can we implement a control scheme as a key management tool?

This session will help grow public awareness on energy conservation issues, in both the industry and the government. This is of key importance to the SC industry in Europe to reduce the industries carbon footprint, and, to reduce the burden from growing energy cost, exposing competitive manufacturing.

SEMICON Europe provides an efficient platform for industry information exchange for shared technology learning towards global industry standards and best practice manufacturing.

Session Co-Chairs

Alfred Koenig, Applied Materials

Christian Pophal, Infineon Technologies

Agenda

- **Introduction: Overview on Committees and Activities in the SC Industry. SEMI Global Care program—Outlook to Form a Benchmark Service**
Sanjay Baliga, SEMI
- **Legislative Regulations: Energy Conservation in EU—Involvement of SC industry—the Role of ICT in Energy Conservation—Regulations and Incentives**
Erastos Filos, European Commission

- **Industry Standards: Energy Conservation Standards (overview, status, targets, roadmap)**
Speaker to be confirmed
- **SC Industry Facilities: High Energy Efficient Wafer Fab Requirements, Status and Future Potentials**
Manfred Renz/Peter Csatory/Michael Aust, M+W Zander
- **OEM Contribution: Eco Efficient Equipment Design and Cost Reductions Potentials: Pareto Analysis, Tool Clustering Concepts, Tool/Facilities Integration**
Shigehito Ibuka, TEL
- **Realization of Cost Reduction Potentials by Applying Eco Efficiency Engineering**
Andreas Neuber, Applied Materials
- **SC Fab/IDM: Energy Conservation in a Semiconductor Fab**
Speaker to be confirmed
- **SC Fab/IDM: Carbon Footprint Reduction Program at ST**
Speaker to be confirmed, STMicroelectronics

Executive Panel

Moderator: Christian Pophal, Infineon Technologies

Who should attend

Fab/Facility Management, EHS Managers, Public Representatives, and related Press

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€150	€250
Non-Members	€200	€250



SEMI Technology Symposium: Metrology and Yield Management

Tuesday, 7 October, 13:30–17:00

ICS—International Congress Center, Stuttgart, Germany

Advanced metrology instrumentation and techniques are crucial for critical dimensions control. Defect detection, data retrieval, modeling methods, root causes defect and failure analysis techniques and correlations jointly determine the progress in yield/productivity learning.

The session Metrology and Yield Management is intended to give more insight into these key enablers for the development and manufacture of increasingly complex semiconductor devices. It covers two parts: In the keynote part international experts from the industry will give overview presentations on current and future requirements for metrology and yield management. The second part consists of submitted papers reporting on latest results concerning ultra shallow junction measurements, three dimensional compositional and structural characterization, defect sampling strategies, and advanced wafer inspection methodology for BEOL.

Agenda

- **Challenges and Opportunities in Integrated Yield Management and Advanced Process Control for Nanometer Era Technologies**
Andrzej J. Strojwas, PDF Solutions, Inc. and Carnegie Mellon University
- **Three-Dimensional Compositional & Structural Characterization of Semiconducting Materials with Sub-nm Resolution**
Stephan Gerstl, Imago Scientific Instruments
- **Full Automated Review File Generation for Defect Sampling Strategies at Infineon using Knights Smart Sampling™**
Andreas Hartmann, Infineon Technologies

- **Accelerate 32 nm Development Cycle with New Wafer Inspection Methodology**

Ellis Chang, KLA-Tencor Corporation

Who should attend

Process and equipment engineers, engineering managers, fab managers, and senior professionals in semiconductor technology and manufacturing

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€150	€250
Non-Members	€200	€250

SEMI Technology Symposium: “More than Moore” Semiconductor Technology

Wednesday, 8 October, 09:00–12:00

ICS—International Congress Center, Stuttgart, Germany

It is now widely recognized that the value of the integrated system lies not only in the powerful digital part of the signal processing, but also in the diversified technologies, which are allowed to interact with the analogue surrounding world and to manage efficiently the power consumption of the system.

These value-added semiconductor technologies were referred as “More-than-Moore” by Europe and the concept is now widely accepted. As the ITRS states “the “More-than-Moore” approach typically allows for the non-digital functionalities [...] to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution.”

This session will first outline the European approach. Examples of semiconductor technologies will then be presented from the relevant fields, including radio-frequency devices, power management subsystems, sensors and actuators, biochips, optoelectronic and imaging devices.

Who should attend

Application developers, semiconductor process and packaging engineers from research and manufacturing

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€150	€250
Non-Members	€200	€250

SEMI Technology Symposium: Lithography/Mask Technology

Wednesday, 8 October, 13:30–17:00

ICS—International Congress Center, Stuttgart, Germany

The imaging capability of sub-wavelength lithography is driven by the enhancement of optical printing technology to an extent that was not anticipated even a few years ago. Conventional ArF 193 nm optical lithography has been pushed down to the 32 nm node using immersion and double patterning. How long and how can this trend be sustained even

further down the roadmap? What are the challenges facing resist systems and mask fabrication? Next Generation Lithography as EUV still needs to resolve numerous technical challenges before being ready for high volume production. Furthermore the increasing complexity of the lithography step raises economical issues. In this context could alternative techniques as imprint or maskless become potential solutions for mainstream applications?

Session Chair

Serge Tedesco, CEA-LETI

Agenda

- **Extending the Horizon of ArF Water-Immersion Lithography: Double Patterning and Related Technologies**
Kazuaki Suzuki, Nikon
- **32 nm Self Aligned Double Patterning for Flash and DRAM**
Jen Shu, Applied Materials
- **Alternative Lithography Techniques (imprint, optical and e-beam maskless)—Niche Applications or Potential for Mainstream Applications?**
Roger Fabian Wedgwood Pease, Stanford University
- **Resist Systems—the Tradeoff between Sensitivity and Resolution/CD Control**
Gronheid Roel, IMEC
- **Mask Fabrication Challenges for the 32 nm Node**
Paul Chipman, Toppan
- **Title to be announced**
Vivek Bakshi, EUVlitho

Who should attend

Technologists, engineers in the lithography/mask area from R&D and manufacturing

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€150	€250
Non-Members	€200	€250



SEMI Technology Symposium: New Materials/Unit Process Steps

Wednesday, 8 October, 13:30–17:00

ICS—International Congress Center, Stuttgart, Germany

Session Co-Chairs

Ivo Raaijmakers, ASM International

Tom Beens, Umicore

Semiconductor innovation is becoming more and more dependent on new materials research. Without these new materials “more Moore” scaling would have stopped already, and “more than Moore” diversification into different functionalities on top of a CMOS baseline would be impossible. In this session, technology leaders from the materials and applications development will present recent progress on groundbreaking materials innovations, ranging from new substrates and Hf-based CMOS gate stacks, to new materials for robust NVMs and nanotube fabrication.

Agenda

- **Atomic Layer Deposition, from R&D into a Multitude of Volume Production Applications**
Jan Willem Maes, ASM Europe
- **Power Dissipation in Doped SbTe Phase Change Material in Memory Cells**
Rob Wolters, NXP
- **Engineered Substrates: Enabling Solutions for “More Moore” and “More than Moore”**
Bruno Ghyselen, Soitec
- **Carbon Nanotubes**
Mike Cook, Oxford Instruments

Who should attend

Process development engineers from the critical materials suppliers and semiconductor process community

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€150	€250
Non-Members	€200	€250

SEMI Technology Symposium: Design for Manufacturing

Thursday, 9 October, 09:00–12:00

ICS—International Congress Center, Stuttgart, Germany

Session Chair

Hugo De Man, IMEC

Semiconductor product cycles—‘time to revenue’—are shortening, while the complexity of devices to be delivered is growing fast. Good DfM (Design for Manufacturing) implementation is crucial to succeed in the very competitive markets; the ability to achieve a ‘first pass success’ is a key asset, which decides on ‘make it or break it’. What are best practices with regards to DfM implementation to ensure ‘verified designs’ and ‘early modeling, process window validation, robust designs’?

SEMICON Europe provides an efficient platform for industry information exchange for shared technology learning towards best practice manufacturing and global industry standards.

This session will shed light on some key DfM issues. Leaders from the design/product development communities are invited to share most recent learnings in advancement in design for manufacturing.

Who should attend

Design/Product Management, Product Engineering, Process Developers, and related Press

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€150	€250
Non-Members	€200	€250

SEMI Technology Symposium: Plastic Electronics

Wednesday, 7 October, 09:00–12:00

ICS—International Congress Center, Stuttgart, Germany

The workshop will be giving an overview of emerging electronic technologies and markets that will facilitate widespread and very low-cost devices. Useful for applications not typically associated with conventional (i.e., silicon-based) electronics -flexible displays, smart labels, animated posters, thin film photovoltaics, active clothing to name a few- the new electronics will find application in new fields due to their expanded capabilities. The result is a forecasted USD\$47 Billion market by 2018. These technologies will have an impact and will also compliment existing technologies, with the semiconductor industry's input necessary in terms of manufacturing, processing and materials.

Agenda

- **Plastic, flexible, printed electronics: Emerging Technologies- Emerging Markets**
Harry Zervos, IDTechEx
- **New possibilities with plastic electronics**
Andreas Tanda, plastic electronic
- **Innovative technologies breathe real life into ordinary paper**
Titus Lindl, Menippos

Who should attend

The workshop should be attended by those interested in entering this competitive market (end users, manufacturers, equipment and materials suppliers) as well as those wanting to keep a close eye on the developments of this burgeoning industry.

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€150	€250
Non-Members	€200	€250

SEMI Standards Workshop: Issues in Measuring Particles in Semiconductor Grade Liquid Chemicals

Tuesday, 7 October, 14:00–17:00

ICS—International Congress Center, Stuttgart, Germany

Session Chair

Gordon Ferrier, Air Products

- | | |
|-------------|---|
| 14:00–14:15 | Welcome and Introduction
Gordon Ferrier, Air Products |
| 14:15–14:40 | Characteristic of the Particle Counter which Influences the Counting Performance
Kaoru Kondo, RION Co. |
| 14:40–15:05 | Entegris' Experience in LPC Measurement Inconsistency
Gunter Haas, Entegris |
| 15:05–15:30 | Liquid Optical Particle Counters: Calibration and Correlation Challenges
Dwight B. Beal, Particle Measuring Systems |
| 15:30–15:55 | Coffee Break |
| 15:55–16:20 | Issues in the Statistical Analysis of Particle Count Data
Thomas J. Bzik, Air Products and Chemicals |
| 16:20–16:45 | Challenges and Problems at the Evaluation of Particles in Liquids
Gummaar De Vos, FujiFilm Electronic Materials |
| 16:45–17:00 | Closing Remarks
Gordon Ferrier, Air Products |

Objective

The measurement of particles in process chemicals and gases creates a number of challenges for the semiconductor industry. For example, different instruments can often provide differing particle measurement data for similar chemical samples. In addition, the traditional

calibration technique using latex spheres in water is likely to be inappropriate for use with typical semiconductor process chemicals, due to significantly differing refractive indices when comparing that of the liquid/particle system under investigation with that of the calibration mixture. Other issues include how to approach the correlation of particle measurement at the point of delivery, with particle size data appropriate to that at the point of use. Measurements are often taken offline but whether this is truly representative can be questionable. Issues also exist with gases and these will also be addressed.

Who should attend

This workshop offers a great opportunity for suppliers and end-users to come together to discuss many challenges and to consider potential solutions to address them.

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€80	€150
Non-Members	€120	€150

Standards Technical Education Program (STEP): SEMI Statistical Guidelines for Ship to Control

Tuesday, 7 October, 09:30–12:30

ICS—International Congress Center, Stuttgart, Germany

- 09:30 **Introduction**
Possible applications for Ship- to-Control limits
Why a standard Ship-to-Control method is necessary
- 09:45 **The Philosophical Principles used to Construct C64-0308**
Changing specifications and the annual clock
Statistical feasibility of Ship-to-Control limits
Fully defined rule sets

10:05	The Key Statistical Methodologies in C64-0308 Control limit estimation Annual review statistical procedures Sample size impact and limitations
11:05	Coffee Break
11:20	Ship-to-Control Software Software Demonstration Examples
12:00	Q&A Session
12:30	Closure of Program

Objective

The new SEMI Standard SEMI C64-0308—*SEMI Statistical Guidelines for Ship-to-Control*, provides a set of guidelines for the quantitative determination of statistically derived limits from process data for the purpose of defining and maintaining Ship-to-Control (STC) limits. There has always been variability in incoming chemical specifications due to inconsistencies in statistical quality control practices in both suppliers and users. To help prevent unproven materials from being shipped, SEMI C64-0308 defines a standard practice for determining ship to control limits. This standardized methodology provides the rigorous control limits that are likely to prove cost effective with broad application of Ship to Control.

The program will provide training with respect to:

- The philosophy underlying the choice of statistical methodologies and associated rule sets utilized in the Ship-to-Control standard.
- Understanding the key statistical methodologies in the standard.
- Using a Windows-based software tool to implement the standard—a FREE CD copy of the software will be given out to all participants of this training program.

What is a STEP?

A Standards Technical Education Program (STEP) is a technical program focused on one or several SEMI International Standards. SEMI produces STEPs to communicate information about newly published or revised

standards, or critical documents under development, that are expected to have a profound impact on industry operations. It is common for members of the originating standards task force to serve as presenters. Attending a STEP will give you the opportunity to learn more about the application of a critical new standard which impacts your manufacturing site or affects your supplier-customer relationships. This technical education program will teach you how to implement new technical information into your everyday fab operations, which may help you and your company to improve your product and processes considerably.

Session Chairs

Tom Bzik, Air Products

Robert Brill, ICL Performance Products

Who should attend

Those who plan to sell or purchase Ship-to-Control grade materials or are involved in the Ship-to-Control chain of impact. On the business side this includes those who market, sell or purchase SEMI grade materials. On the technical side this includes those involved with the measurement and monitoring of SEMI grade materials (quality and process control professionals and management, analytical professionals and management). Production engineers either producing or consuming Ship-to-Control product will benefit from understanding what this standard does and does not do.

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€150	€250
Non-Members	€200	€250

Standards Technical Education Program (STEP): EHS Guidelines for Semiconductor Manufacturing Equipment (SEMI S2/S8)

Thursday, 9 October, 08:30–12:30

ICS—International Congress Center, Stuttgart, Germany

- 08:30 **Introduction**
Bert Planting, ASML
- 08:40 **Session on SEMI S8**
Mark Harralson, Intel
SEMI S8 Introduction:
What MMH activities have to be assessed?
Overview of standard MMH analysis tools
- 08:50 **1991 NIOSH equation**
Data collection and analysis
Example problem
- 09:20 **Biomechanical Analysis**
Data collection and analysis
Example problem
- 09:50 **Psychophysical Analysis**
Data collection and analysis
Example problem
- 10:10 **Risk Characterization of Non-Compliant
Situations**
Future S8 enhancements
Recommended references
- 10:20 **Coffee Break**
- 10:40 **Session on SEMI S2**
Saranpal Rai, Intertek
SEMI S2 Introduction:
SEMI S2 and other related SEMI S
Documents
SEMI S2 and its relation to regulatory
requirements
- 10:50 **Design for Safety: Electro-mechanical
Hazards, Electrical Design, Interlocks
and Emergency Shutdown, Robotics &
Automation**

11:20	Design for Safety: Physical Hazards Ionizing/Non-Ionizing Radiation, Lasers and Noise Earthquake, Labeling & Documentation
11:40	Design for Safety: Chemical Hazards Chemicals, Ventilation and Environmental
12:00	Design for Fire Safety: Fire Protection and Heated Chemical Baths
12:10	Q&A Session Moderator: Bert Planting, ASML
12:30	Closure of Program

Objective

As far as ergonomics risks are concerned, the majority of design issues today relate to maintenance and service activities and the most prevalent concern in these types of tasks are the handling of heavy equipment components. The training will cover the three most common MMH assessment methods expected to be performed as part of an S8 assessment, and will touch on recommended risk characterization for non-compliant tasks.

SEMI S2 is the most widely accepted basic industry safety guidelines used to design Semiconductor Manufacturing Equipment (SME). It consists of specific requirements for several types of hazards associated with SME, including electrical, mechanical, chemical, lasers and radiations. As the basic design guide for the SME it also has significant impact on the regulatory requirements around the world. This course will provide you with the basic understanding of the SEMI S2 requirements and their relationship to other regulatory standards around the world.

What is a STEP?

A Standards Technical Education Program (STEP) is a technical program focused on one or several SEMI International Standards. SEMI produces STEPs to communicate information about newly published or revised standards, or critical documents under development, that are expected to have a profound impact on industry operations. It is common for members of the originating standards task force to serve as presenters. Attending a

STEP will give you the opportunity to learn more about the application of a critical new standard which impacts your manufacturing site or affects your supplier-customer relationships. This technical education program will teach you how to implement new technical information into your everyday fab operations, which may help you and your company to improve your product and processes considerably.

Session Chairs

Mark Harralson, Intel
Saranpal (Sunny) Rai, Intertek
Bert Planting, ASML

Who should attend

Individuals involved in the design or EHS evaluation of semiconductor manufacturing equipment.

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€150	€250
Non-Members	€200	€250

Safety of Machinery Seminar: “Introduction to *EN IEC 62061* and *EN ISO 13849*”

Wednesday, 8 October, 08:30–13:45 (22:00 including social program)

Pilz GmbH & Co. KG, Felix-Wankel-Str. 2, 73760 Ostfildern, Germany

08:30–09:00	Transfer by shuttle from New Messe Stuttgart (exhibition entrance) to Pilz Automation in Ostfildern + Security Check in
09:00–10:45	Safety of Machinery Seminar—Part 1 Introduction to <i>EN IEC 62061</i> and <i>EN ISO 13849</i>
10:45–11:00	Coffee Break
11:00–11:30	Pilz Automation Company Tour

	“Turning Semiconductors into Safety Controls”
11:30–13:15	Safety of Machinery Seminar – Part 2 Machinery Safety for the Semiconductor Industry
13:15–13:45	Lunch Break
13:45–14:30	Transfer to the Mercedes Museum
14:30–16:45	Mercedes Museum Tour
17:00–22:00	Volksfest (walking distance from Mercedes Museum). Note: Transfer back from the Volksfest is up to each individual attendee.

Objective

The aim of this one-day introductory level course is to equip delegates with information on the scope and main design requirements these standards promote and to give an appreciation of how to apply their principles.

By the end of the course delegates will have:

- Been given an insight into the need for competence in the design of safety related control systems and how this should be addressed.
- Have gained an awareness of the key parts of the EN 62061 standard including SIL determination, diagnostic coverage and Common Cause Failures etc, for safety circuit designs.
- Have gained an understanding of the differences between BSEN 954-4 and pr EN ISO 13849-1 and the concepts which the new standard promotes, including the determination and justification of performance levels rather than safety categories.

Who should attend

The course is aimed at managers, technicians and design engineers who have responsibilities for machinery safety-related control systems.

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€80	€150
Non-Members	€120	€150

7th Silicon Wafer Standards Workshop: "Si Wafer Trends and Requirements for Solar and Semiconductor Devices"

Wednesday, 8 October, 09:00–13:00

ICS—International Congress Center, Stuttgart, Germany

- 09:00–09:10 **Welcome and Introduction**
- 09:10–09:35 **Joining Forces for Standardization—An Opportunity to Make PV Economically Sustainable**
Wolfgang Koch, KoSolCo
Werner Bergholz, Jacobs University Bremen
Bettina Weiss, SEMI
- 09:35–10:00 **Ultrapak® Edge Guard 200mm Wafer Shipper**
Jorgen Lundgren, Entegris
- 10:00–10:25 **SOI Material Readiness for 22 nm Technology Node**
Christophe Maleville, Soitec
- 10:25–10:40 **Coffee Break**
- 10:40–11:05 **Chucked Wafer Flatness in the Next Generation**
Tetsuo Fukuda, Fujitsu Microelectronics
- 11:05–11:30 **450mm Silicon Wafer Development—A Status Update**
Michael Goldstein, Intel Corporation
- 11:30–11:55 **Chemical Bulk Analysis of Silicon**
Anton Huber, GeMeTec Metrology
- 11:55–12:20 **Impact of Wafer Quality on Efficiency of PV Cells**
Speaker Invited
- 12:20–12:45 **Edge Defects**
Speaker Invited
- 12:45–13:00 **Closing Remarks**

Objective

The workshop aims to inform the semiconductor community about future silicon wafer developments and potential standardization needs. Future technology generations will require increasingly perfect and optimized Si Wafers, challenging manufacturing processes as well as related metrology. This includes bare Si Wafers as well as wafers with functional layers. Standardization with respect to wafer parameters as well as metrology for establishing a common understanding and language regarding these issues would benefit the entire semiconductor industry.

This year's workshop will be targeting both the semiconductor and photovoltaic industries.

Semiconductor Industry Topics will include 450mm wafers status update, defects and particles on silicon wafer edge and an update on silicon-on-insulator (SOI) and strained-Si wafers. *Photovoltaic Industry Topics* will include Poly-Si versus refined Silicon, relationship of material properties and solar cell efficiency, advanced Solar Cells and Industry Standards activity update.

Session Chairs

Peter Wagner

Werner Bergholz, Jacobs University Bremen

Laszlo Fabry, Wacker

Who should attend

Device/Cell manufacturers, silicon wafer suppliers, equipment suppliers, and R&D organizations

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€80	€150
Non-Members	€120	€150

Silver Sponsor



10th European Manufacturing Test Conference (EMTC)

Tuesday, 7 October, 09:00–18:00

ICS—International Congress Centre Stuttgart, Germany

Conference Chairs

Davide Appello, STMicroelectronics

Martin Stadler, Teradyne

- 09:00–09:05 **Welcome by EMTC Committee Chair**
Davide Appello, STMicroelectronics
- 09:05–09:15 Opening Remarks
- 09:15–10:00 **Keynote: Test Implications of the ITRS
Roadmap**
Roger Barth, Numonyx

Session I: “Package Test”

Session Chair

to be appointed

- 10:00–10:25 **Laser Direct Testing of IC Package
Substrates**
Laurence Pujol, Beamind
- 10:25–10:50 **Test Sockets—Addressing the Challenges
of Leadfree Packages**
Gerhard Gschwendtberger, Multitest
- 10:50–11:15 **Memory Test Sockets on the Move—from
Spring Probes to PCR**
Joachim Moerbt, Advantest
- 11:15–11:40 **Coffee break**

Session II: “Adaptive Test”

Session Chair

René Segers, NXP Semiconductors

- 11:40–12:05 **Technology Innovations Enable Vastly
Improved Test Quality**
John Bearden, Optimal Test
- 12:05–12:30 **A Test Cell Control Architecture for Multiple
External System Interfaces**
Steve Ledford, Verigy
- 12:30–12:55 **Adaptive Test at NXP**
René Segers, NXP Semiconductors
Dan Glotter, Optimal Test
- 12:55–14:00 **Lunch**

Session III: "Test Engineering Challenges"

Session Chair

Martin Stadler, Teradyne

14:00–14:25 **Cost Of Test (COT) Improvement—How to Keep Pace with the Current Test Challenges**

Stephane Mougin, STMicroelectronics

14:25–14:50 **TPG (Test Program Generator)—Generating a Full Test Program for a New Device in One Hour**

Christian Bonnin, ATMEL Rousset.

Bob Whyte, Credence Systems Corp.

14:50–15:15 **Parallel RF Wafer Sort Production Testing**

Frank Goh Heng Huat, Verigy

Tan Eng Keong, Verigy

15:15–15:45 **Coffee Break**

Session IV: "The all days challenge: Probe cards and contacts/sockets"

Session Chair

Klaus-Detlef Paesch, AMD

15:45–16:10 **NXP**

16:10–16:35 **Infineon Technologies**

16:35–17:00 To be announced

17:00–17:45 **Panel Discussion: Influence of ITRS on the Future of Tests in Europe**

Moderator: René Segers, NXP Semiconductors

17:45–18:00 **Closing Remarks**

18:00–20:00 **SEMICON Europa International Reception**

Who should attend

Manufacturing test floor managers, experts, R&D counterparts and the key representatives of test equipment and service companies

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€300	€500
Non-Members	€400	€500

Platinum Sponsors



Advanced Packaging Conference “Technologies, Manufacturing and Supply Chain”

Wednesday, 8 October, 13:00–18:15

Thursday, 9 October, 09:00–12:30

ICS—International Congress Centre, Stuttgart, Germany

Europe continues to be at the forefront of Advanced Packaging Technologies for the semiconductor industry as it is home to leading chip makers, equipment manufacturers and material producers. In conjunction with Europe's world famous Institutional Centers of Excellence in chip design and technology development, European industry provides the insight into what will become the next generation processes to be adopted in the emerging applications requiring enabling chip packaging technology.

SEMICON Europa once again hosts the annual Advanced Packaging Conference, which this year will focus on the latest emerging technologies around Through Silicon Via (TSV), Wafer Level Packaging (WLP) and Embedded Die manufacturing processes. The conference will have one session focusing on the manufacturing, processes and materials needed to support the implementation of advanced packaging, as well a second session focusing on the enabling technology and applications. In addition there will be a high profile “Executive Summit” panel discussion looking at the issues of the supply chain; and how, in Europe, it can support and benefit from, the development of these new technologies.

The target audience is chip design engineers, device packaging engineers, assembly equipment makers, materials suppliers and business managers who need to know the issues involved with design, development and incorporation of emerging technology devices into system based equipment and products. The conference sessions will be held over two days.

Agenda

Wednesday, 8 October (Day 1 of 2)

13:00–13:10 **Opening and Welcome Introduction**
Conference Chair: Andy Longford, Panda Europe (Chair of IMAPS UK)

Session I **Advanced Manufacturing, Processes & Materials**

13:10–13:45 **Keynote: Future Packaging Scenarios for Cell Phones**

Nils Lundberg, Sony Ericsson Mobile Communications

13:45–14:10 **Bumping for WLCSP using Micro Solder Ball Attach on Electroless NiAu and NiPdAu UBM**

Thomas Oppert, Pac Tech

14:10–14:35 **TLS—Wafer Dicing Don't Saw Away Your Profit!**
Hans-Ulrich Zühlke, Jenoptik Automatisierungstechnik

14:35–15:00 **High Aspect Ratio through Wafer via Metallization by Highly Ionized Sputtering**

Jürgen Weichart, OC Oerlikon Balzers

15:00–15:30 **Coffee break**

15:30–15:55 **A Cost Efficient IC Separation Technology Ultra Tight Scribe Lanes by Laser Dicing**

Guido Albermann, NXP Semiconductors
Roland Schneider, NXP Semiconductors

15:55–16:20 **Embedded High-K Thin Film Capacitor in Organic Package**

Hironori Tanaka, Ibiden Co.

16:20–16:45 **PIQC-System (Process-integrated Quality-control)**

Rolf Beckert, Hesse & Knipps

Session II **Embedded Die & Wafer Level Packaging**

16:45–17:05 **Keynote: Kauppi Kujala, Nokia**

17:05–18:15 **Panel Discussion**

Wafer Level Packaging & Embedded Die Supply Chain—Who will be the ones to do it?

Moderator: Françoise von Trapp, Managing Editor, *Advanced Packaging* magazine

test, assembly and advanced packaging

Panel Executives:

- Kauppi Kujala, Nokia, representing the OEM
- Eef Bagerman, NXP, representing the IDM
- Andreas Dill, Oerlikon Balzers, representing the equipment supplier
- Hironori Tanaka, Ibiden Co., representing the substrate manufacturer
- A key person from Industry, representing the foundry
- A key person from Industry, representing the packaging subcontractor

18:15–19:00 **Reception**

Thursday, 9 October (Day 2 of 2)

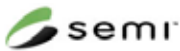
- 09:00–09:05 Welcome to Day 2—More on Embedded Die and WLP
Conference Chair: Andy Longford—
PandA Europe/IMAPS UK
- 09:05–09:40 **Guest Speaker:**
From MEMS to Smart Systems Integration
Thomas Gessner, Fraunhofer Research
Institution for Electronic Nano Systems
- 09:40–10:05 **3D IC & TSV, A Market Overview**
Jean-Christophe Eloy, Yole Développement
Eric Mounier, Yole Développement
- 10:05–10:30 **High Aspect Ratio through Wafer via
Metallization by Highly Ionized Sputtering**
Jean Michailos, STMicroelectronics
- 10:30–11:00 **Coffee break**
- 11:00–11:25 **Embedded Die Technology, Next Generation
Packaging for Discrete Semiconductors**
Wil Peels, NXP Semiconductors
- 11:25–11:50 **Recent Developments in WLB and eWLB
Technology**
Thorsten Meyer, Infineon
- 11:50–12:15 **High Density 3D Die Stacking without
Through-Si-Vias: Ultra Thin Chip
Embedding as Enabling Technology**
Eric Beyne, IMEC
- 12:15–12:30 **Closing remarks**

Who should attend

Advanced Packaging experts, manufacturing and R&D counterparts and the key representatives of packaging equipment and service companies

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€300	€500
IMAPS Members	€300	€500
Non-Members	€400	€500

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SEMI Technology Arena—Exhibitor Presentations: Test, Assembly, Advanced Packaging/MEMS

Wednesday, 8 October, 10:30–13:00

The SEMI Technology Arena is located in Hall 1 with a seating capacity of 80. Exhibitors will make presentations on their latest products and innovations. Attendance is FREE. See detailed agenda on page 53.



International MEMS/MST Industry Forum

Monday, 6 October, 09:30–18:15

Mövenpick Hotel, Stuttgart Airport, Germany

“Challenges and Opportunities in the MEMS Industry”

This year’s forum will give an overview on the challenges and opportunities in MEMS industry. Key players of the industry have been invited to present their perspectives and to share experiences on the MEMS market. The sessions will be organized under the following four topics:

- **MEMS manufacturing industry**
Leading MEMS manufacturers will give their view on the evolution of the MEMS business in different market sectors including consumer, automotive, energy and biotech.
- **MEMS wafer processes**
MEMS equipment manufacturers and research institutes will present new trends in MEMS wafer processing including wafer bonding and dicing.
- **MEMS packaging, inspection and testing**
Focus will be on hermetic packaging and new inspection and test methods.
- **MEMS markets**
Short presentations from leading MEMS market research companies will be followed by an open discussion of trends in the MEMS market.

Agenda

- 09:30–09:35 **Opening Remarks by Heinz Kundert,
President, SEMI Europe**
- 09:35–09:40 **Welcome by Conference Committee Chairman
Felix Rudolf, CTO, Colibrys**

Session I: MEMS Manufacturing Industry

Session Chair

Jérémie Bouchaud, iSuppli

09:40–10:10 **Keynote: Rob O’Reilly, Analog Devices**

- 10:10–10:30 **MEMS on 200mm**
Andreas Wild, Freescale
- 10:30–10:50 **Gyroscope System Design for Automotive Applications**
Guido Dupont, Melexis
- 10:50–11:20 **Coffee break**
- 11:20–11:40 **QPatch—A Commercial BIOMEMS Application**
Simon Pedersen, Sophion Bioscience
- 11:40–12:00 **MEMS Accelerometers for Seismic Applications**
Felix Rudolf, Colibrys
- 12:00–12:20 **Standardized and Robust MEMS Foundry Processes Revolutionize Commercialization of MEMS**
Tomas Bauer, Silex Microsystems
- 12:20–13:20 **Lunch break**

Session II: MEMS Wafer Processes

Session Chair

Christian Schaefer, PVA Tepla

- 13:20–13:40 **Bonding with Al Metallurgies**
Shari Farrens, Suss MicroTec
- 13:40–14:00 **Electrical Vias for 3D MEMS on Wafer Level**
Thomas Hoefftmann, Plan Optik
- 14:00–14:20 **CMP—An Enabling Technology for MEMS Fabrication**
Gerfried Zwicker, Fraunhofer Institute for Silicon Technology ISIT
- 14:20–14:40 **Aspects of PVD Metal Film Stress Control for MEMS Device Metallization**
Paul Werbaneth, Tegal Corporation
- 14:40–15:00 **The Challenge of Dicing MEMS Structures**
Peter Lange, Fraunhofer Institute for Silicon Technology ISIT
- 15:00–15:20 **TLS-Dicing – A Now Technology for MEMS Packaging**
Hans-Ulrich Zuehlke, Jenoptik
Automatisierungstechnik

micro-electro-mechanical systems MEMS/MST

15:20–15:40 **Coffee break**

Session III: MEMS Packaging and Testing

Session Chair

Peter ten Berge, ASML

15:40–16:00 **New Strategies for Final Test of Multiple MEMS Sensor Types within One Package**

Andreas Nagy, Multitest

16:00–16:20 **New Developments in High Throughput Scanning Acoustic Microscopy for Automated Inspection of Bonded Wafers**

Peter Czurratis, SAM TEC

16:20–16:40 **Digital Holography Microscopy (DHM) for Static and Dynamical 3D Characterization MEMS and Moems**

Yves Emery, Lyncée Tec

16:40–17:00 **Versatile Low-Cost Water Level Packaging Enabled by Powerblasting**

James Lee, Applied Microengineering

17:00–17:20 **Multi Site Test and Simulation of MEMS Devices**

Frank Grossmann, SPEA

Session IV: MEMS market

Session Chair

Uwe Schwarz, X-Fab

17:20–17:30 **MEMS Market and Industry 2007—2012**

Jérémie Bouchaud, iSuppli

17:30–17:40 **MEMS Market Overview**

Jean-Christophe Eloy, Yole Développement

17:40–18:15 **Q&A—Wrap-up and Closing Remarks**

Chair: Felix Rudolf, CTO, Colibrys

18:15–19:00 **Reception**

Who should attend

MEMS/MST companies and R&D institutions, with their equipment, materials and service providers, will get great opportunities for their managers and professionals to network and share learning in technology and market developments for successful MEMS/MST production strategies.

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€300	€500
Non-Members	€400	€500

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SEMI Standards: MEMS Technical Committee

Tuesday, 7 October, 09:00–13:00

ICS—International Congress Center, Stuttgart, Germany

Price: FREE

SEMI Standards: 3D Metrology for MEMS Task Force

Tuesday, 7 October, 14:00–17:00

ICS—International Congress Center, Stuttgart, Germany

Price: FREE

SEMI Technology Arena—Exhibitor Presentations: Test, Assembly, Advanced Packaging / MEMS

Wednesday, 8 October, 10:30–13:00

The SEMI Technology Arena is located in Hall 1 with a seating capacity of 80. Exhibitors will make presentations on their latest products and innovations. Attendance is

Price: FREE:

See detailed agenda on page 53.

4th Advanced Photovoltaic Manufacturing Technology Conference

Wednesday, 8 October, 13:30–18:00

Thursday, 9 October, 09:00–12:00

ICS—International Congress Center, Stuttgart, Germany

The 4th Photovoltaic Manufacturing Technology Conference will take the issues mentioned at the last Fab Managers Forum in Dresden, and present solutions from the equipment and the materials suppliers. Fab Managers want access to the latest technology possibilities, have full control on their production process, and have flexible and sustainable facilities in order to drive down the unit costs of each wafer, cell or module produced. This year a balanced program is offered, offering new technology development, latest research results, tools that enable ASPC in photovoltaics, and the latest development in recycling and sustainable facilities.

The target audience is facility managers; chief engineers or purchase managers of wafer manufacturers; cell or module makers and any other important stakeholders in the PV industry who are concerned with the latest developments and issues in PV manufacturing.

The conference is split in two segments over two half days: Day One will focus on new technologies, while Day Two concentrates on productivity, yield improvement, manufacturing excellence and sustainable facilities.



Agenda

Wednesday, 8 October

Session I: PV Technologies

- **Keynote: Opportunities for the PV industry in Transports**
Pietro Perlo, Senior Scientist and Director, Centro Ricerche Fiat
- **Emerging High-efficiency Technologies for Industrial Solar Cell Production**
Jochen Rentsch, Head of Group "Wet Chemical & Plasma Technologies/Process Transfer", Fraunhofer ISE
- **Crystalline Si Solar Cells: The Quest for Thinner Cells**
Kris Baert, Program Manager Solar Cells, IMEC
- **Structuring of Thin Film Solar Cells**
Gabriele Eberhardt, Head of Application, Jenoptik Automatisierungstechnik
- **Solar Concentrator Cell from Semiconductor Scrap**
Rainer Krause, Manager Technology Centre, IBM
- **New Inline Cluster Tool Concept for Silicon TF PV Modules**
Rudolf Beckmann, Project Manager R&D Solar II, Leybold Optics
Ortrun Wiechers, Project Manager, Fraunhofer IPA
- **Laser Systems & Processes within Next Generation Photovoltaic Manufacturing Equipment**
Finlay Colville, Director of Marketing - Solar, Coherent
- **New Materials for Elastomeric Seals to Address New Materials Being Used in Semiconductor Devices**
John Foggiano, Technical Marketing Manager, Greene Tweed

Thursday, 9 October

Session II: Manufacturing Excellence and Sustainable Facilities

- **Improved TCO Layer Deposition using Novel DC Power Supplies**
Dirk Ochs, Senior Application Engineer, Hüttinger Elektronik + Co.
- **Advanced Process & Equipment Control in Photovoltaic Industry and their Benefits**
Maxim Zagrebnov, Applications Manager, PDF Solutions

photovoltaic

- **Ingot Cost Reduction and Wafer Efficiency Optimization by means of Numerical Simulations of Crystal Growth Processes**
Arnaud de Potter, Technical Sales Engineer, FEMAGSoft
- **Scaling Factors for High Volume PV Manufacturing Facilities**
Peter Csatory, Vice President Manufacturing Technology Group, M+W Zander FE
- **Water Treatment and Sustainable Development in the Photovoltaic Industry**
Maria Rosaria Lapalucci, Marketing Manager, Nalco Italiana

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€300	€500
Non-Members	€400	€500

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SEMI Technology Arena—Exhibitor Presentations: Photovoltaic

Tuesday, 7 October, 14:00–17:00

SEMI Technology Arena—Hall 1

The SEMI Technology Arena is located in Hall 1 with a seating capacity of 80. Exhibitors will make presentations on their latest products and innovations. Attendance is FREE. See detailed agenda on page 53.



SEMICON Europa—Executive Summit “MADE IN EUROPE”

Tuesday, 7 October, 16:30–17:45 (followed by Awards and International Reception)

ICS—International Congress Center, Stuttgart, Germany

Timely availability of leading edge hi-tech products is essential in the very competitive environment of major global markets. For Europe to remain in leadership positions in our key industrial sectors such as automotive, telecommunication, machinery, medical etc; we must be prepared, that product differentiation is determined by innovative microelectronics. Executive industry leaders will debate on how to best leverage R&D and Microelectronics “Made in Europe” for maintaining a leadership in Europe’s key, successful industry sectors.

2008 Panel: Invited Executives from Microelectronics Makers, Users and R&D

- Valentin von Tils, VP, Bosch Automotive Electronics
- Hans-Jürgen Straub, CEO, X-Fab
- Heinz Gerhäuser, Chairman of the Board of Dir. Microelectronics Alliance Fraunhofer
- Luc Van Den Hove, COO, IMEC
- Malcolm Penn, CEO, Future Horizons

Panel Chair:

Heinz Kundert, President, SEMI Europe

Who should attend

Senior executives from SEMI member companies, device manufacturers, and industry stakeholders

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€150	€250
Non-Members	€200	€250

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SEMICON Europa—International Reception

Tuesday, 7 October, 18:00–19:30

ICS—International Congress Center, Stuttgart, Germany

The International Reception is the annual networking gathering of exhibitors, their customers and stakeholders at SEMICON Europa. It is the ideal place to connect with industry leaders from around the world. Decision-makers representing the semiconductor and related industries, plus equipment, material and service suppliers, gather to exchange views over a buffet dinner in a relaxed, casual atmosphere. This event is not to be missed for its invaluable networking opportunities—a real chance to be able to cultivate productive relationships.

This year, the International Reception will also play host to the SEMI Europe Awards and the International SEMI Standard Awards.

Who should attend

Senior executives from SEMI member companies, device manufacturers, and industry stakeholders

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€75	€120
Non-Members	€100	€120



IC Industry Awards comes to Europe!

The Awards will be presented in Europe this year on 7 October at SEMICON Europa 2008.

12th Fab Managers Forum

Monday, 6 October, 15:15–21:30: Visit of the BOSCH Reutlingen Technology Mfg. Site & Dinner Reception

Tuesday, 7 October, 09:00–13:30: Forum & Lunch
Bosch, Mövenpick & ICS—International Congress Center, Stuttgart, Germany

The 12th European Fab Managers Forum will be presented by Semiconductor Equipment and Materials International (SEMI), in co-operation with the BOSCH Reutlingen Management team.

This conference has become a respected meeting venue for fab managers, executives and professionals from the European semiconductor industry to meet and discuss topics that are of mutual interest in the essential drive towards “Total Productivity” in semiconductor manufacturing.

To take full advantage of the opportunity to mix with other attendees, we are planning a reception on Monday evening at the “Mövenpick Airport Hotel” following a company-visit to the BOSCH Reutlingen technology site, with its upcoming new Semiconductor fab and new test facilities, on Monday afternoon.

The forum presentation and panel sessions are scheduled for Tuesday morning—the first SEMICON Europa 2008 show—allowing an efficient travel schedule should you wish to visit both events.

The SEMICON Europa 2008 Executive Panel/International Reception on Tuesday afternoon is another interesting networking opportunity for FMF attendees, who plan to stay until Wednesday.

How to Get a Lean Semiconductor Fab, fit for Purpose, and Most Efficiently Running; 200 and 300mm Prime!

Fab managers, executives, and industry experts will discuss topics of the essential ‘total productivity’ drive.

Enhancements for 'Given' and New Fabs/Maximized Equipment Utilization & Overall Line Efficiency

The pressure for continued productivity improvements is relentless; in the current business environment it is crucial that S/C manufacturers identify all sensible efficiency gains to maintain tight cost management.

Key opportunities for increased productivity need to be understood and must be leveraged in order to maximize the bottom line ROI on MFG Assets—releasing much needed capital for further investments.

Monday, 6 October

- 15:15 Shuttle Bus at “Stuttgart Airport meeting point” to the BOSCH Reutlingen site
- 16:00–17:00 Visit of the BOSCH Reutlingen Technology manufacturing site
- 17:15 Shuttle Bus from BOSCH Reutlingen to the New Mövenpick Airport Hotel
- 18:30–21:30 Dinner Reception, at the “New Mövenpick Hotel” at Stuttgart Airport

Tuesday, 7 October

- 07:30–08:30 Registration
- 09:00–11:00 FMF Presentation Session
- 11:00–12:00 FMF Executive Panel Session (AMD, Bosch, Infineon, ST, Numonyx, NXP, Renesas, etc, invited)
- 12:00–13:30 Lunch

Who should attend

European fab management and related executives and professionals from the semiconductor industry

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€200	€320
Non-Members	€260	€320

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Market Briefing

Tuesday, 7 October, 08:30–11:00

ICS—International Congress Center, Stuttgart, Germany

The SEMI Market Briefing will provide reliable and timely market information, forecasts and expert analysis to help business planning. Speakers will present on the worldwide semiconductor market outlook, semiconductor capital equipment and materials markets, and photovoltaic market development.

Agenda

- **SEMI Equipment and Materials Outlook**
Dan Tracy, SEMI
- **Is there Light at the End of the Chip Market Tunnel?**
Malcolm Penn, Future Horizons
- **Market for Critical Subsystems and Components used in semi and related Manufacturing Equipment**
John West, VLSI Research Europe
- **Trends in (Advanced) Packaging Technologies**
Andy Longford, PandA Europe
- **MEMS Market Briefing**
Jérémie Bouchaud, iSuppli Corporation
- **Markets for Plastic and Printed Electronics**
Harry Zervos, IDTechEx
- **Photovoltaic Market Briefing**
Jean-Christophe Eloy, Yole Développement

Who should attend

Professionals in sales, marketing, business development, finance, consulting, product planning, investors and analysts

Price	Valid through 19 September	Beginning 20 September
SEMI Members	€150	€250
Non-Members	€200	€250

SEMI International Standards Program



SEMI®
International
Standards

SEMICON Europa Standards Meetings

Today, the SEMI Standards portfolio is considered one of the key services offered to the industry—providing standards and safety guidelines that are timely, critical, and of immense economic value. SEMI is continuously broadening the scope and reach of the International Standards Program by strategically expanding standards-related activities into new markets and new technology areas.

The major accomplishments of our time are increasingly achieved through collaboration.

Like a fine Swiss watch, each component may be a perfect expression of form and function, but it is synchronized effort that enables their ultimate purpose. Standards, particularly in our capital and technology-intensive industry, are a critical component to the essential collaborations that must be achieved to create new markets and move existing markets forward efficiently and profitably.

The SEMI International Standards Program brings experts from the semiconductor, flat panel display, MEMS, nanotechnology, photovoltaic, and related industries together to exchange ideas and work jointly to develop globally accepted technical standards. The results of this activity enable positive growth and economic benefit to the industries that SEMI serves. SEMI Standards contribute to faster commercialization and time-to-market, especially for new and emerging technologies.

The SEMI International Standards Program, established in 1973, covers all aspects of semiconductor process equipment and materials, from wafer manufacturing to test, assembly and packaging, display

manufacturing, and now emerging technologies such as nanotechnology, and MEMS/MST. Standards provide a global approach for applying consensus-based solutions and include specifications, test methods, terminology standards and safety guidelines for the semiconductor and related industries. More than 740 SEMI Standards have been published to address critical manufacturing challenges for factory automation, environment, health and safety (EHS), substrates and metrics for manufacturing efficiency. Collectively, SEMI Standards have enabled the efficient proliferation of global wafer fab development and saved the industry billions of dollars.

SEMI has relied on thousands of industry volunteers worldwide to help develop a wide range of International Standards. Approximately 1,500 volunteer experts representing 630 companies work in 17 global technical committees and over 200 task forces to find solutions to technology challenges.

All meetings take place from 7 to 9 October. Standards task force and technical committee meetings are open to all interested parties at no charge. Meeting agendas and schedules are available at www.semiconeuropa.org/standards.

The following meetings will be held in conjunction with SEMICON Europa 2008:

Automation

- Equipment Automation Standards Technical Committee
- Sensor Actuator Network Communication Standard for PROfinet (SANPRO) Task Force

Materials

- Gases and Liquid Chemicals Standards Technical Committee
- Precursors Specification Task Force
- Joint ITRS—SEMI Meeting
- Compound Silicon Materials Standards Technical Committee

SEMI International Standards Program

- GaAs Wafer Specification Standards Task Force
- SiC Wafer Specifications Standards Task Force
- Contactless Capacitive Resistivity and Mobility Task Force
- Carbon in GaAs Standards Task Force

- Silicon Wafer Standards Technical Committee
- Advanced Wafer Geometry Standards Task Force
- Automatic Surface Inspection Standards Task Force

Environment, Health & Safety

- Environment, Health & Safety Standards Technical Committee

MEMS (Micro-Electro-Mechanical Systems)

- MEMS Standards Technical Committee
- 3D Metrology for MEMS Task Force

Awards

The SEMI International Standards Award 2008 will be held during the International Reception

(See SEMICON Europa International Reception on Tuesday, 7 October, 17:30–19:30)

How Can I Join the SEMI Standards Program?

Participation in the SEMI International Standards Program is open to all. SEMI underwrites the costs of administering the program as a service to the industry. Meetings are open and anyone may attend. Members may join one or more technical committees as voting or non-voting members by filling out a simple application form. Visit us at www.semi.org/standards for more information.

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Visit www.semiconeuropa.org/standards for agendas and other details

SEMI Technology Arena








“49% of SEMICON Europa visitors come to discover new products and technologies.”

The SEMI Technology Arena is located on the show floor in Hall 1 with a seating capacity of 80. Exhibitors will make presentations on their latest products and innovations. Attendance is FREE.

Tuesday 7 October 2008

10:30	SEMI Membership Video	
10:45	SEMI market statistics presentation on MEMS	<u>MEMS</u>
11:00	MEMS exhibitor presentation	
11:15	Xactix presentation on MEMS	
11:45	“Temporary Bonding Enables TSV and 3D-Technology with Ultra-Thin Substrates” by Stefan Pargfrieder, EVG	
12:00	“Recent Advances in Silicon DRIE for MEMS Manufacturing” by David Haynes, STS	
12:15	“Anhydrous HF Vapor Technology for Stiction Free MEMS Release” by Paul Hammond, Primaxx	
12:30	“Focus Ion Beam Technologies for MEMS Prototyping and Processes” by Francis Morrissey, FEI	
13:15-14:00	Lithography/Inspection exhibitor presentation	<u>Lithography</u>
13:15	“Application of the Focused Electron and Ion Beam Devices in Nanotechnologies” by Martin Zadrazil, Tescan	
13:30	“New Approach for Full-Field Nano Imprint Lithography” by Johann Weixlberger, Suss MicroTec	
14:15	SEMI statistics presentation on Photovoltaic	<u>Photovoltaic</u>

SEMI Technology Arena

- 14:30-14:45 Photovoltaic exhibitor presentation
- 14:45 “Recent Developments in High Throughput Scribing Systems for Thin Film Photovoltaics” by Dave Clark,
Newport Spectra-Physics 
- 15:00 “Examples of Industrial Community Research Projects for Photovoltaic Applications” by Volker Sittering, **Fraunhofer Institute for Surface Engineering and Thin Films** 
- 15:15 “FFEM Contribution to the PV Industry” by Geert Duchesne, **FUJIFILM Electronic Materials** 
- 15:30 “Power Supplies for PV Applications” by Dirk Ochs, **Huettinger Elektronik** 
- 15:45 “MES in the Photovoltaic - A System for the Whole Supply Chain from Silicium to Module” by Ricco Walter, **AIS Automation Dresden** 
- 16:00 “Multi-Level Large Scale Photovoltaic Production Facilities” by Philipp Neff, **MW-Zanders** 
- 16:15 “Focused Ion Beam Technologies for High Volume Analyses and Reliability Testing for Photovoltaics and Film Stacks” by Francis Morrisey, **FEI** 

Wednesday 8 October 2008




- 10:30 SEMI Membership Video
- 10:45 SEMI market statistics presentation on final manufacturing [Packaging](#)
- 11:00 “Hybrid Packaging Technology Development by CSEM in the framework of IntegramPlus” by

	Christian Bosshard, CSEM	
11:15	“High Resolution DRIE and Ultra-High Aspect Ratio Resist for TSV and 3D Packaging” by Michael Stan, MicroChem Corp.	
11:30	“Advanced Bonding and Lithography Technologies for Wafer-Level 3D Integration and CIS Packaging” by Markus Wimplinger, EVG	
11:45	“Advances in DRIE Technology for 200mm and 300mm Wafer Through Silicon Via (TSU) Applications” by David Hayes, STS	
12:00	Exhibitor Packaging presentation – open slot	
12:15	“3D Integration Using Wafer-to-Wafer Bonding for TSVs” by Margarete Zoberbier, Suss MicroTec	
12:30	Test exhibitor presentation	<u>Test</u>
12:45	“New Benchmarks in Final Test” by Multitest	
13:00	“Test Sockets for Best Cost of Test” by Multitest	
	Lunch sponsored by Multitest	
13:30-14:30	Automation exhibitor presentation	<u>Automation</u>
13:45	Automation presentation by Markus Thamm, Ricmar Sales & Services	
14:00	“Next Generation Solution for Improved Fab Efficiency” by Jayakrishnan Nair, L&T Infotech	
15:00-17:00	Second hand Equipment: A Global Perspective Organized by SEC/N and SEMI. Co-sponsored by the following SEC/N Member Companies:	<u>Refurbished Equipment</u>



SEMI Technology Arena

Thursday 9 October 2008

10:30	SEMI Membership Video	
10:45-11:15	R&D Science Park institute presentation	<u>Science Park</u>
11:15	Fraunhofer IZM (Institute for Reliability and Microintegration) presentation	
11:30	IMEC presentation	
11:45	Presentation by Didier Louis, CEA-LETI  Leti  	
12:00	“Hybrid Chipscale Integration for Inertial Sensor Clusters” by Stephan Warnat, Fraunhofer ISIT (Institute for Silicon Technology)	
12:15	“Accelerating Innovation in Semiconductor R&D” by Richard Visser, MiPlaza , Philips Research	
12:30-13:15	R&D Science Park institute presentation	<u>Associations</u>
13:30	“SEMI: Mobilizing Europe’s Strengths” by Carlos Lee, SEMI	
13:45	Industry Association presentation, JEMI France	
14:00	“Cool Silicon solutions from Saxony - Silicon Saxony - The Leading European Network and its Visions” by Heinz Martin Esser, Silicon Saxony	
14:15	“IVAM - B2B accelerator for micro, nano and materials” by Uwe Kleinkes / Christine Neuy, IVAM Microtechnology Network	
14:30	“VDMA Productronic: Networking the German Electronics Production Equipment Industry” by Sabine Egerer, VDMA Productronic	
14:45	“Performance Improvement Through Knowledge Networks” by David Law, NMI	
15:00	“Creating business opportunities in the UK” by Iain Hyslop / Mike Smyth, JEMI Director, JEMI	

Science Park “MADE IN EUROPE”

Dedicated area on the show floor

Research and development is one of Europe’s strengths. World leading ideas, patents and processes would not be possible without the tremendous influence of several institutes in Europe. SEMICON Europa 2008 will focus on this track in a special way.

In a move to promote the global advancement of R&D, SEMI is adding the “Science Park” to its line-up of exhibits and will provide research institutions and start-up companies with a platform for introducing new products and services to the semiconductor market. In the spotlight will be a new hybrid car developed by the Fraunhofer IISB. In addition to the exhibition on the show floor, Science Park sessions are integrated into the Technology Arena. The Science Park session delivers seminar-style presentations, designed to provide exhibitors with an additional platform to engage and share product developments with an international audience.

“Research, technology, and innovation are key drivers for economic growth and sustainable development. The Science Park at SEMICON Europa will be our platform to demonstrate the potential of R&D in Europe and will provide opportunities for collaborative efforts between our researchers and the international community.”

– Prof. Heiner Ryssel, Fraunhofer IISB

Science Park “MADE IN EUROPE”

“The semiconductor industry is under continued cost pressure and moving away from Europe to the Far East: thus, endangering, in the long term, the R&D capacity still existing in Europe to support production. To ensure the large public European efforts in R&D the direct interest of the semiconductor industry is helping the industry remain competitive and viable. Communication between researchers and the industry must be intensified to align the strategic priorities. The Science Park at SEMICON Europe is an excellent opportunity for exchange and collaboration between the research community and industry to help strengthen Europe’s position in the global semiconductor industry.”

– Matthias Krieger, CSEM



Fraunhofer Institut
Integrierte Systeme und
Bauelementetechnologie



Fraunhofer Institut
Siliziumtechnologie



Fraunhofer Institut
Zuverlässigkeit und
Mikrointegration



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By Car—The New Stuttgart Trade Fair Centre is directly connected to the A8 motorway and the B27 (1 hour 50 minutes from Frankfurt airport; 2 hours from Munich airport)

By Plane—Stuttgart airport terminals are 200m from the new Trade Fair Centre. There is a direct connection via S-Bahn (S2 and S3) to Stuttgart central station. Travel time: 27 minutes.

Frankfurt airport is 1 hour 14 minutes from Stuttgart's main railway station.

By Train—Stuttgart's main railway station is located 13Km from the new Trade Fair Centre. Rapid-transit trains (S-Bahn) leave Stuttgart main station every 10 or 20 minutes.

SEMICON[®] *Europa*2008

Dates

Exhibition: 7–9 October 2008

Programs and Events: 6–9 October 2008

Exhibition opening hours

7–8 October 2008—10:00-17:00

9 October 2008—10:00-16:00

Location

New Stuttgart Trade Fair Centre &
International Congress Centre Stuttgart (ICS)

12,000 pre-registered visitors

600 exhibitors

Organizer



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